Avances en Mezcladores: Circuitos Subarmonicos y sus Aplicaciones

Carlos E. Saavedra, Ph.D.
Profesor Asociado y
Coordinador de Postgrado
Electrical and Computer Engineering
Queen's University
CANADA

Plan de la charla

- Porque los mezcladores subarmonicos?
- Mezcladores subharmonicos (SHM) en CMOS
- Análisis del SHM basado en la celda de Gilbert-Cell
- Avances recientes: el SHM con multiplicación x4
- Multiplicadores de frequencia usando SHM's
- Conclusión

CMOS Subharmonic Mixers and Applications

Gigahertz Integrated Circuits Group

Líder del grupo y diseñador en jefe:

Profesor Carlos Saavedra

Estudiantes de doctorado

Ahmed El-Gabaly, Jiangtao Xu

Maestria:

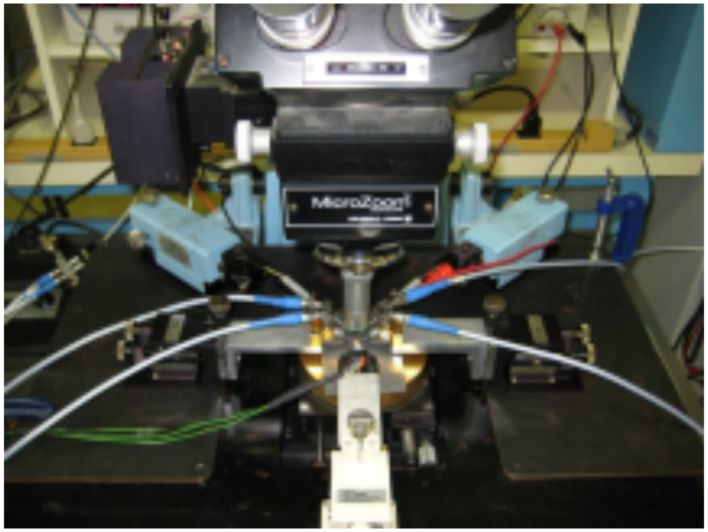
Min Wang, Shan He

Pregrado

Greg Reynen, Jeet Mondal, Kevin Greig

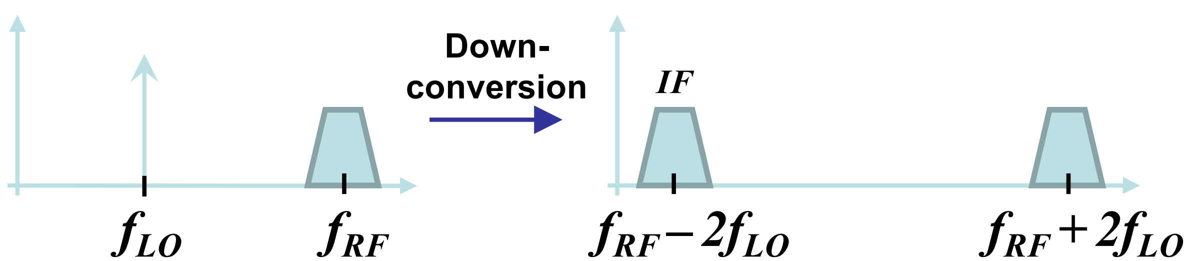
Infraestructura Experimental

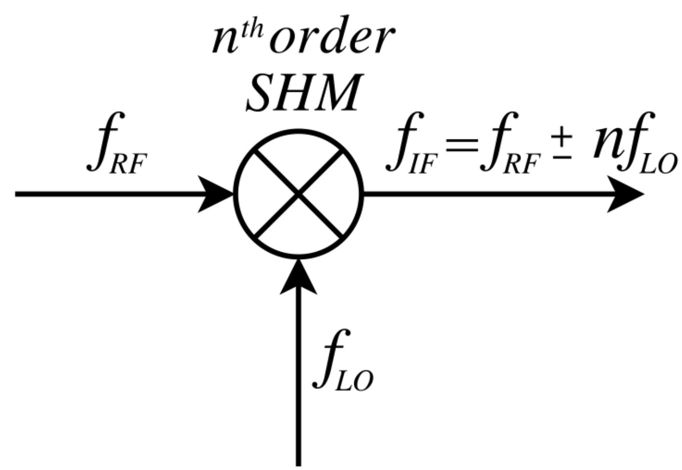
- Probe Station
- 50 GHz Vector Network Analyzer
- 44 GHz Spectrum Analyzer with Noise Fig. measurement capability
- 40 GHz Signal Generators (Anritsu)
- Digital Sampling Oscilloscopes



Subharmonic Mixers – the "big picture"

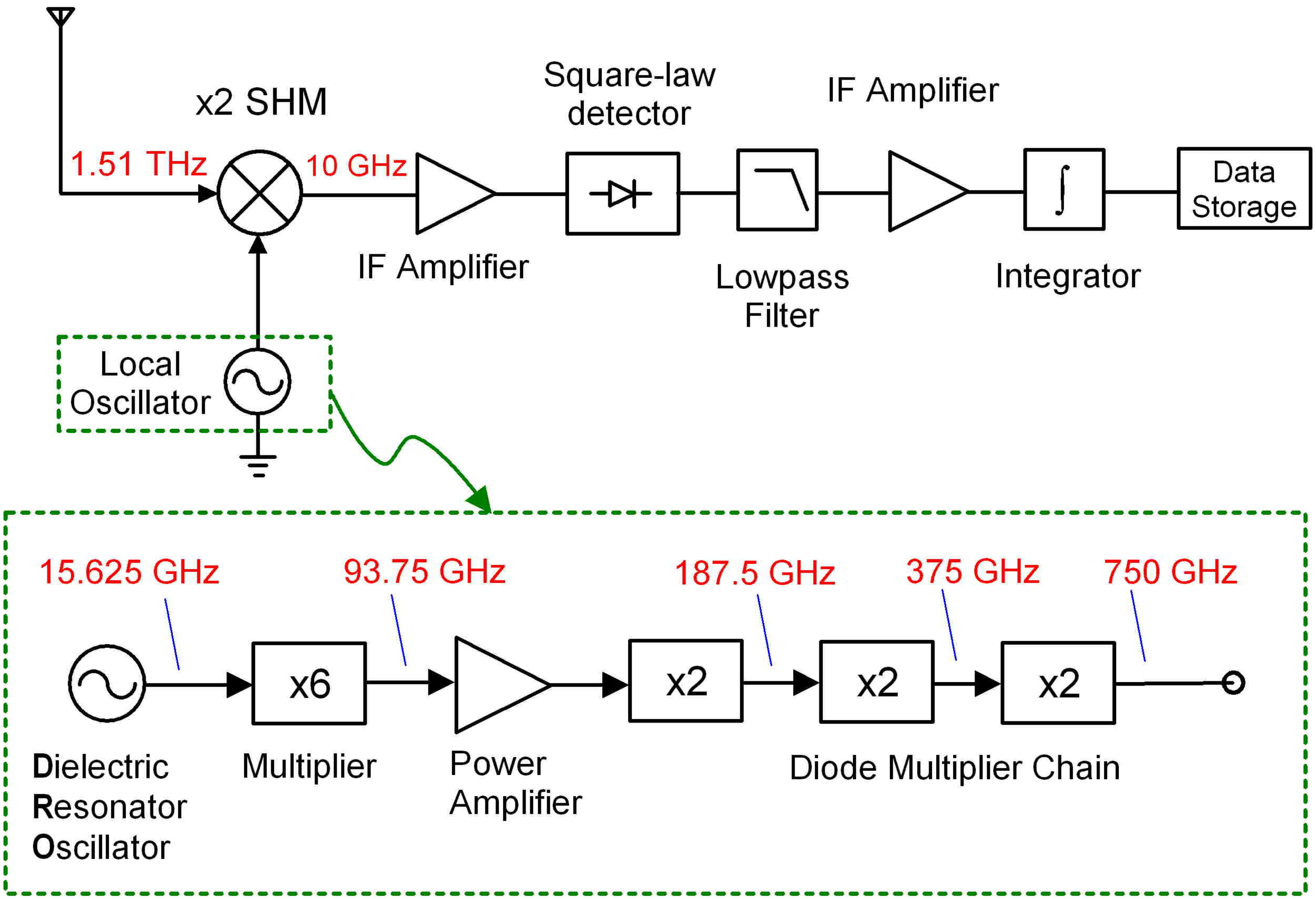
- Output signal frequency is the sum and difference of one input frequency and a multiple of the other input frequency.
  - Internally multiplies f_{LO}





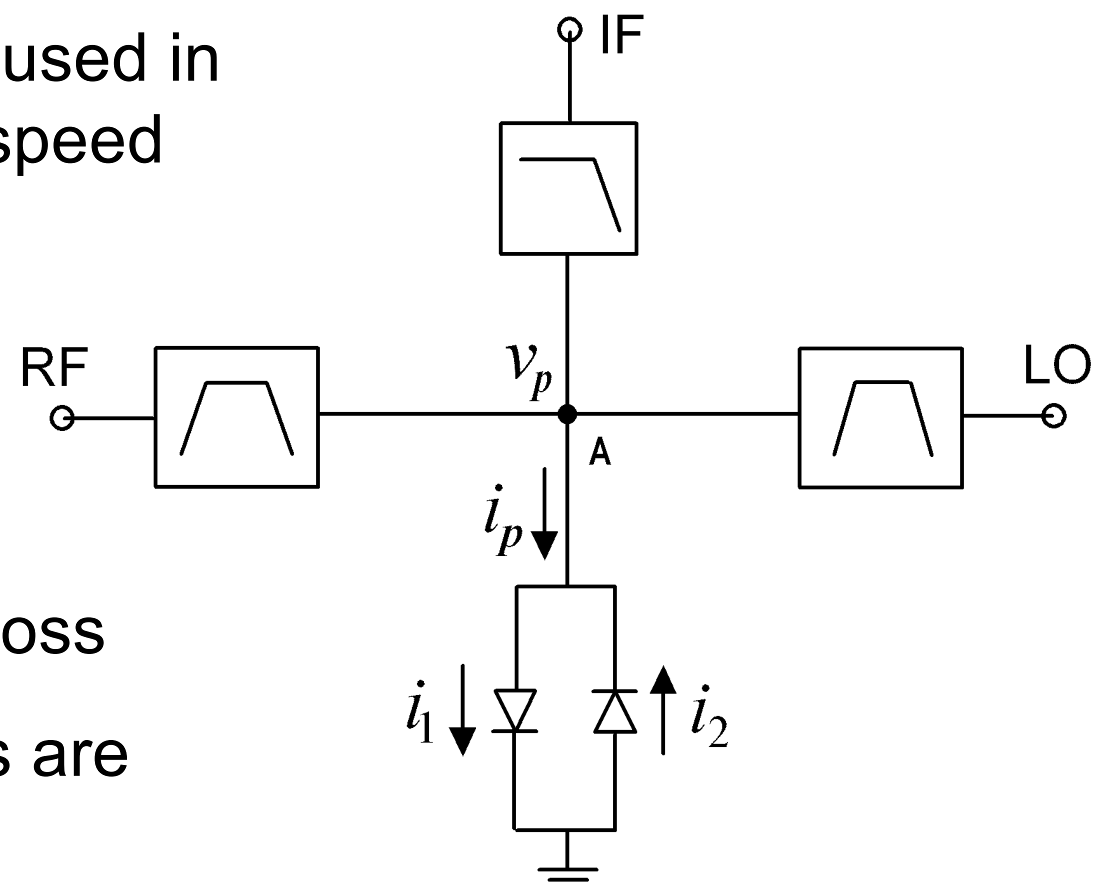
2x SHM → $n=2$ 4x SHM → $n=4$

Terahertz Receiver for Radio Astronomy

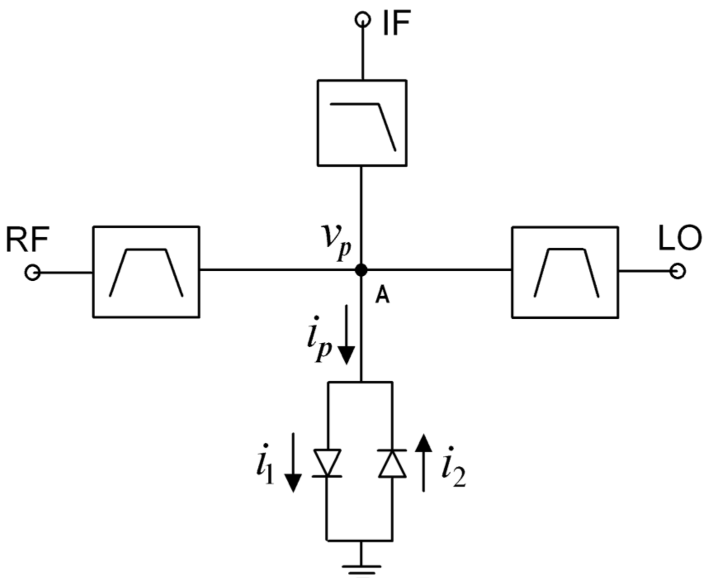


Diode-based Subharmonic Mixers

- Schottky diodes are often used in THz systems due to their speed
- The mixers are cooled to 4 Kelvin to minimize their internal noise
- Waveguide structures are preferred due to their low loss
- Mixers using SIS junctions are also employed



Diode SHM analysis



$$v_p = A_{rf}\cos(\omega_{rf}t) + A_{lo}\cos(\omega_{lo}t)$$

The currents are:

$$i_1 = I_o\left(e^{v_p/nV_T} - 1\right) \quad \text{and} \quad i_2 = I_o\left(e^{-v_p/nV_T} - 1\right)$$

Summation at node v_p:

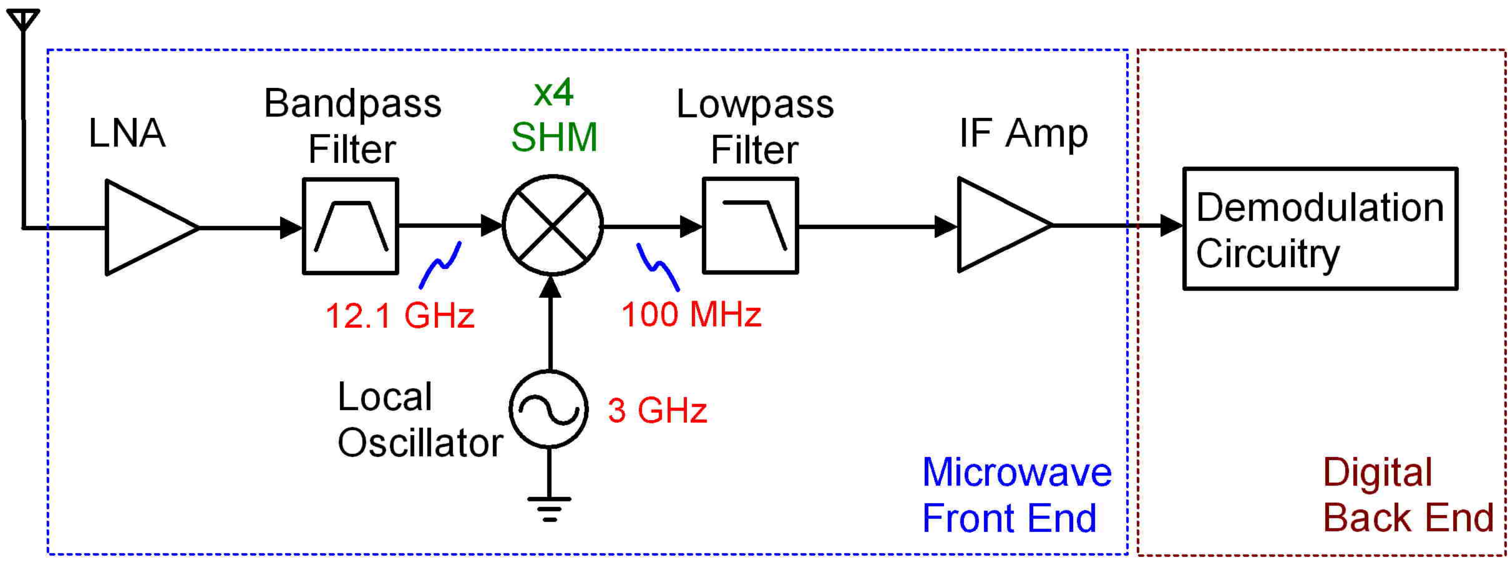
$$i_p = I_o\left(e^{v_p/nV_T} - e^{-v_p/nV_T}\right)$$

Taylor series expansion:

$$i_p = I_o\left[2\left(\frac{v_p}{nV_T}\right) + \frac{1}{3}\left(\frac{v_p}{nV_T}\right)^3\right]$$

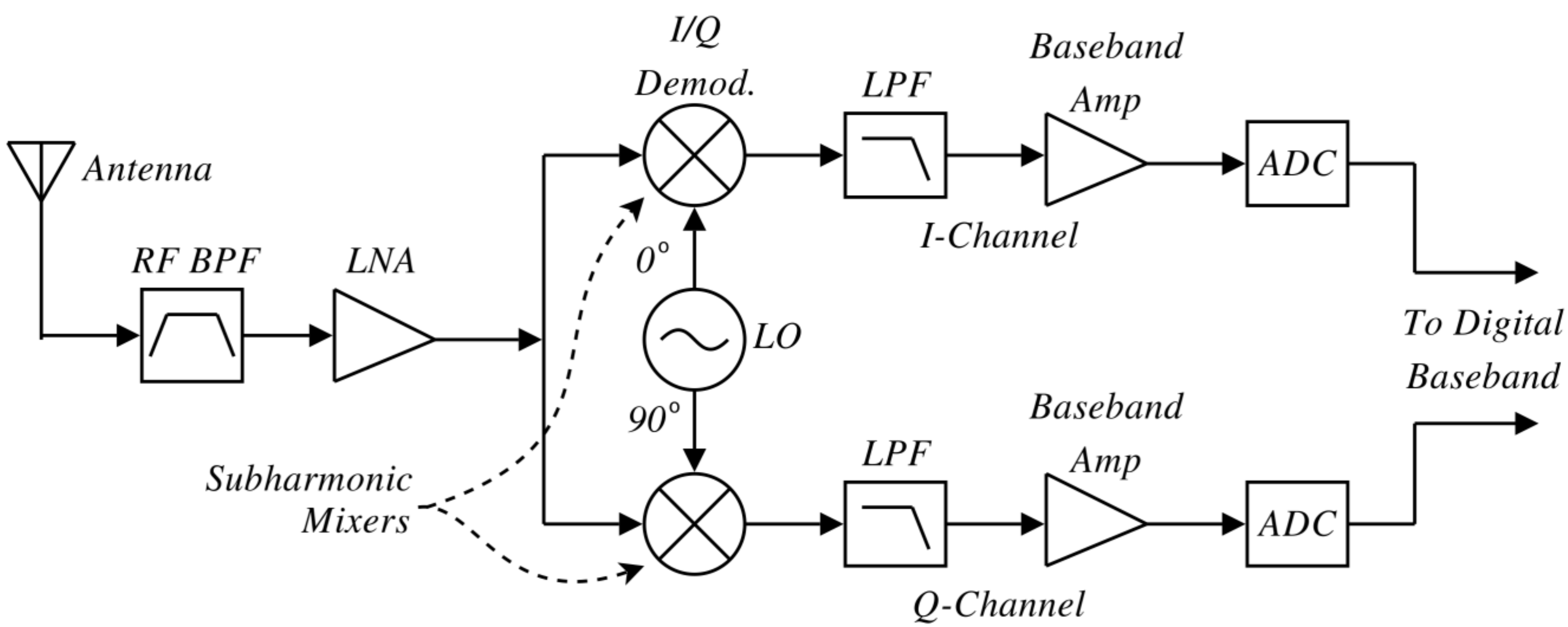
one of the multiplication terms is: $(1/4n^3V_T^3)A_{rf}A_{lo}^2\cos(\omega_{rf} \pm 2\omega_{lo})t$

SHM's in Superheterodyne Receivers



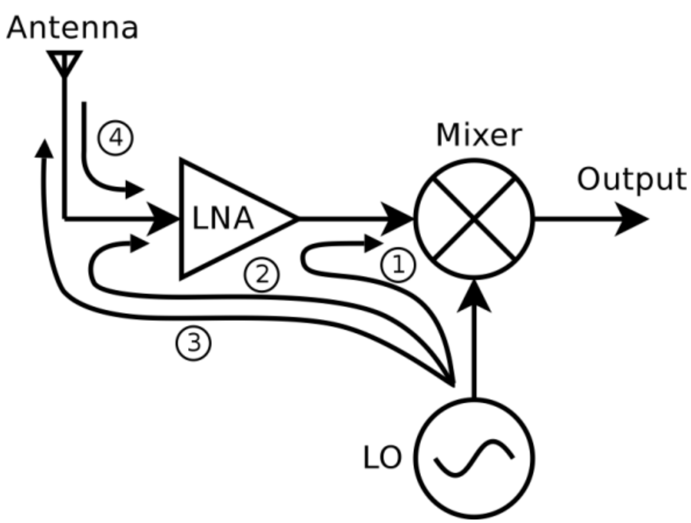
- The LO frequency is reduced by f_{LO}/n
- Oscillator phase-noise is much better at lower frequencies than at higher ones. At 3 GHz one could use an FBAR resonator and get a XTAL oscillator performance levels

Direct-Conversion (zero IF) Receivers



LO self-mixing in a fundamental mixer cause serious interference problems at baseband in direct-conversion receivers

LO self-mixing in zero-IF receivers



$A_{LO}\cos(\omega_{LO}t)$

using a fundamental mixer:

$$A_{LO}\cos(\omega_{LO}t)A_{FT}\cos(\omega_{LO}t) = \frac{1}{2}A_{LO}A_{FT} + \frac{1}{2}A_{LO}A_{FT}\cos(2\omega_{LO}t)$$

baseband signal

using a x2 Subharmonic mixer:

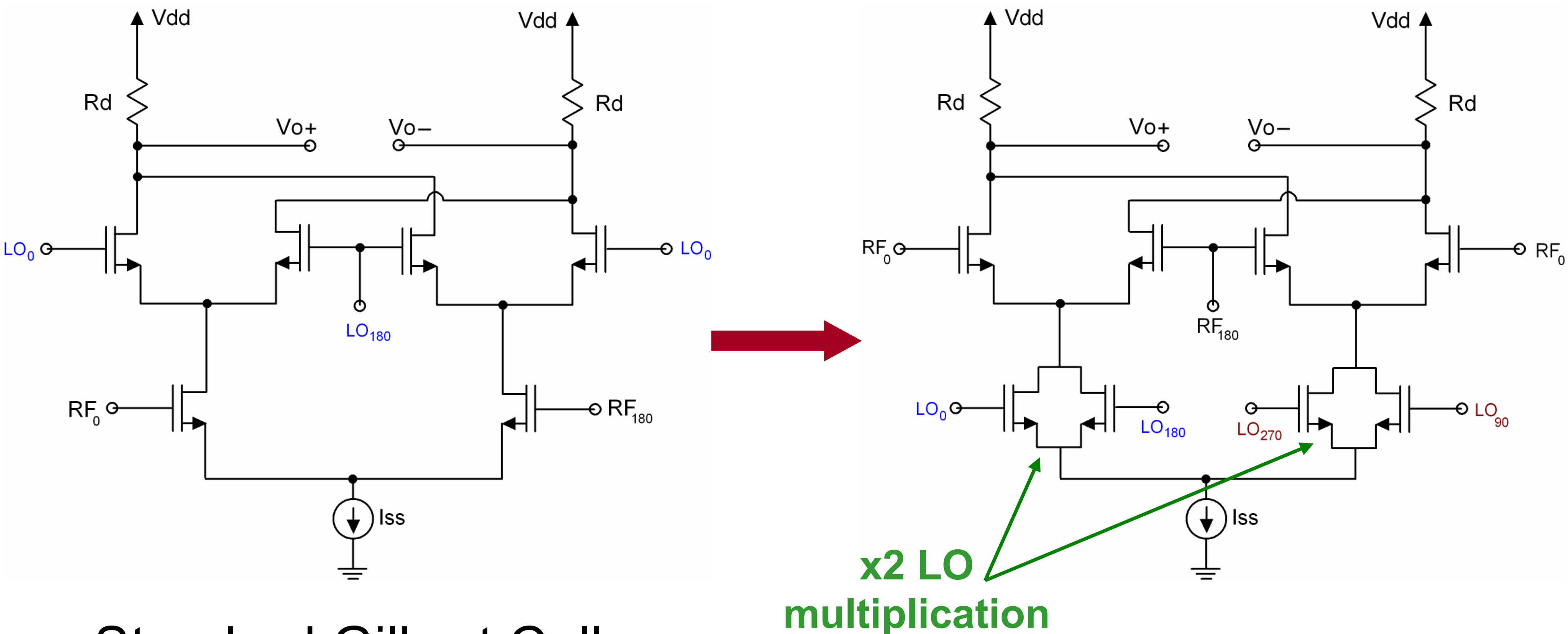
self-mixing products are **not at baseband**

$$A_{LO}\cos(\omega_{LO}t)A_{FT}\cos(2\omega_{LO}t) = \frac{1}{2}A_{LO}A_{FT}\cos(\omega_{LO}t) + \frac{1}{2}A_{LO}A_{FT}\cos(3\omega_{LO}t)$$

CMOS SHM Design Considerations

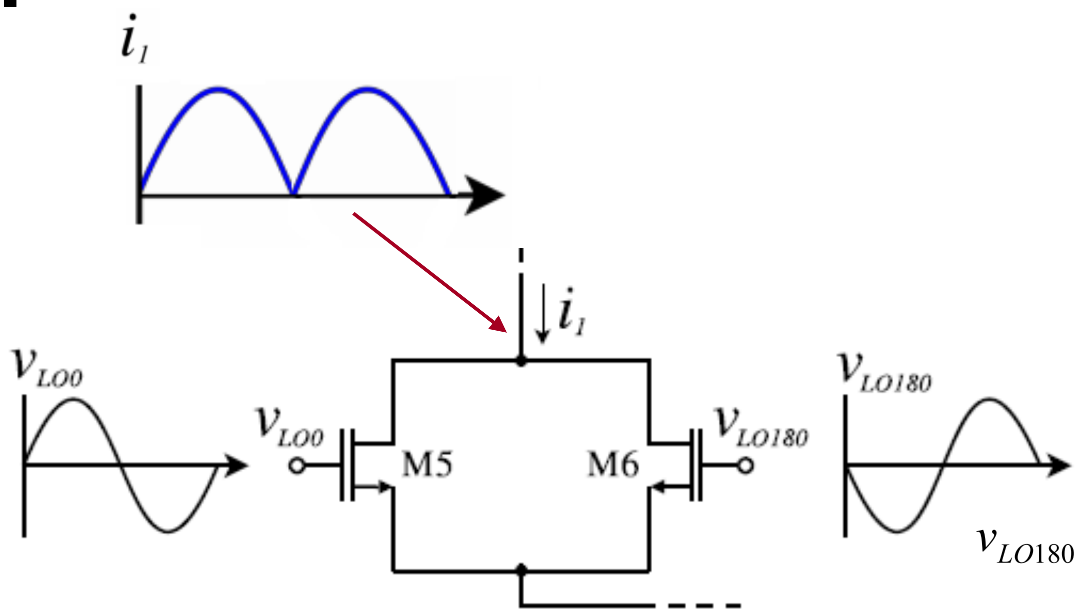
- SHM's based on the Gilbert cell have **conversion gain**, even at high multiplication factors
- **High port-to-port isolation** is easily achieved using a differential circuit topology
- In contrast to diode-based SHM's, **diplexers are not needed** to feed the RF and LO signals to the mixer
- These attributes, however, come at the cost of DC power consumption and lower P_{1dB} and IIP3 relative to diode-based SHM's.

x2 SHM using a Gilbert Cell [3-5]



Standard Gilbert Cell

x2 SHM Operation Details



$$v_{LO0} = A_{LO}\sin(\omega_{LO}t)$$

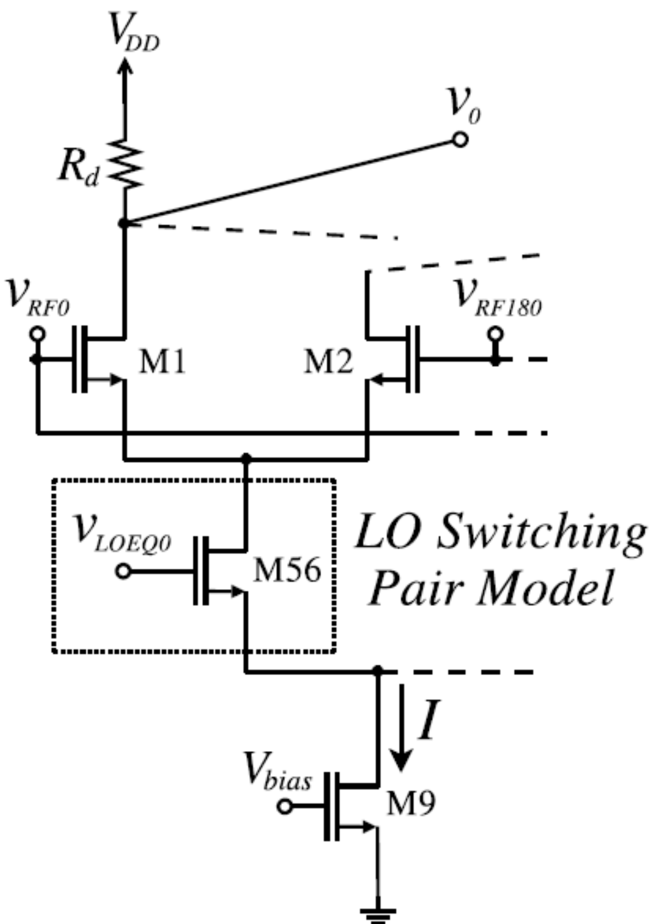
$$v_{LO180} = A_{LO}\sin(\omega_{LO}t - \pi)$$

$$i_1 = i_a + i_b = \mu_n C_{ox}\frac{W_1}{L}(V_{GS(LO)} - V_t)^2 + \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L}(v_{LO0}^2 + v_{LO180}^2)$$

$$i_1 = \mu_n C_{ox}\frac{W_1}{L}(V_{GS(LO)} - V_t)^2 + \mu_n C_{ox}\frac{W_1}{L}v_{LO0}^2$$

Using the relationship, $v_{LO0}^2 = v_{LO180}^2$

Modeling the Conversion Gain

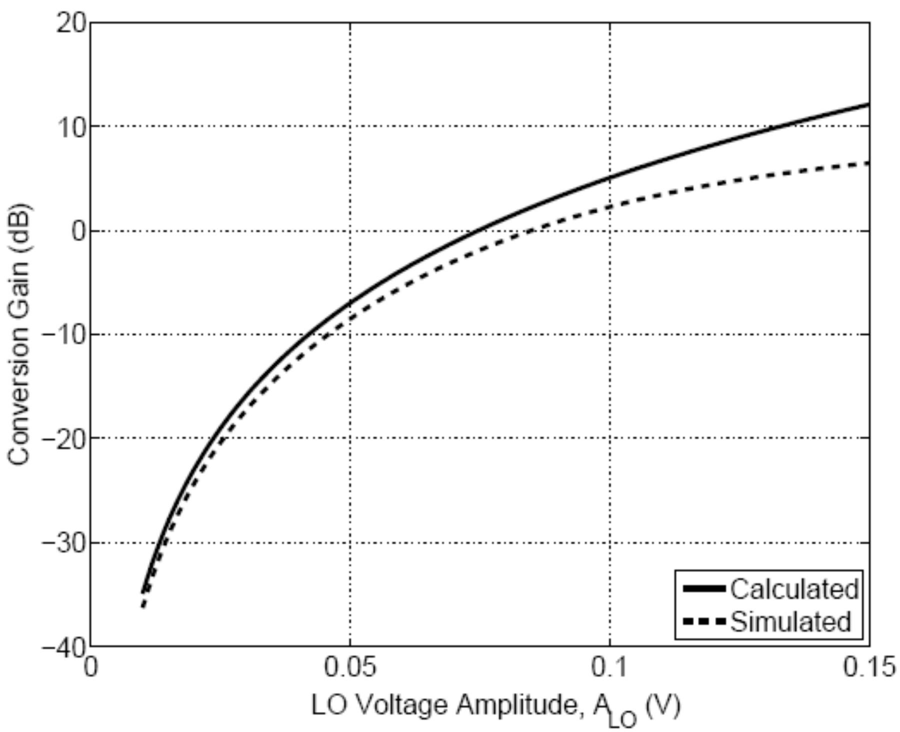


- Converge the two transistors in the X2 doubler network into a *single equivalent* transistor
- The drive signal of the equivalent transistor is,

$$v_{LOeq} \propto \cos(2\omega_{LO}t)$$

- Analyze the resulting mixer circuit as a classic Gilbert-Cell mixer to obtain a a closed-form expression for conversion gain.

Modeling the Conversion Gain – cont'd



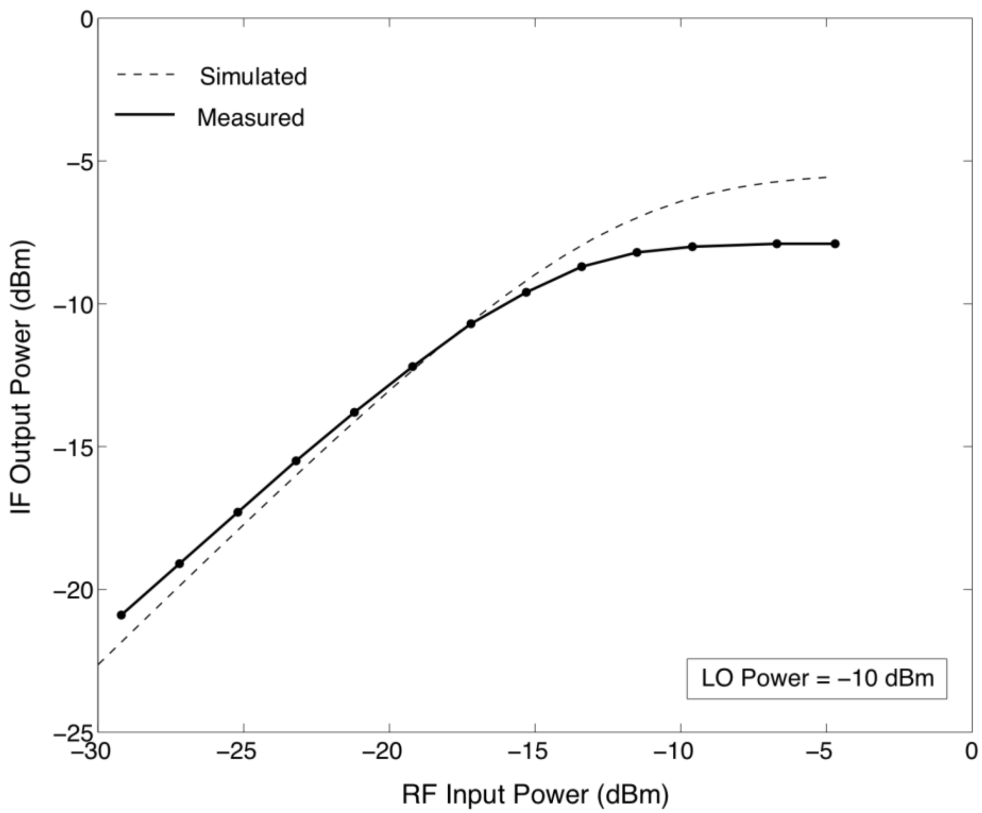
$$v_{LOEQ0} \approx \frac{A_{LO}^2}{4(V_{GS(LO)} - V_t)} cos(2\omega_{LO}t)$$

$$v_{LOEQ180} \approx \frac{A_{LO}^2}{4(V_{GS(LO)} - V_t)} cos(2\omega_{LO}t + \pi)$$

$$CG_{dB} = 20log\left(\frac{R_d I A_{LO}^2}{4(V_{GS(RF)} - V_t)(V_{GS(LO)} - V_t)^2}\right)$$

For more modeling details see Ref. [6]

CMOS x2 SHM Power Performance

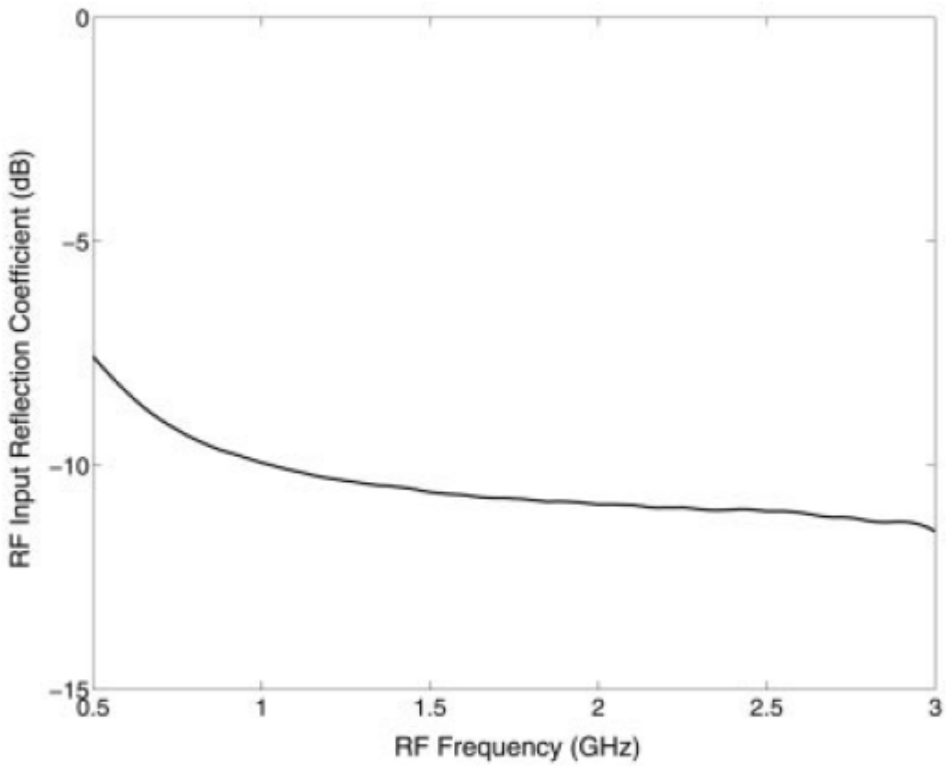


Conversion Gain ~ 8 dB

$P_{1dB,out}$ = - 9 dBm

OIP3 = 0 dBm

RF input match

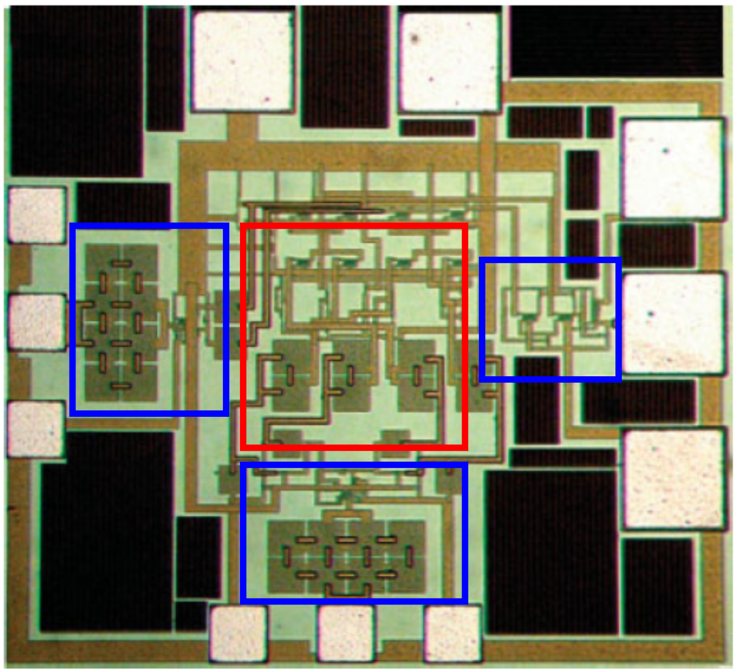


Broadband input match obtained using an active balun at the RF port

Port Isolations

Ports	*Isolation*
RF–LO	62 dB
LO–RF	58 dB
2LO–RF	68 dB
RF–IF	35 dB
LO–IF	37 dB
2LO–IF	49 dB

x2 SHM Chip Microphotograph



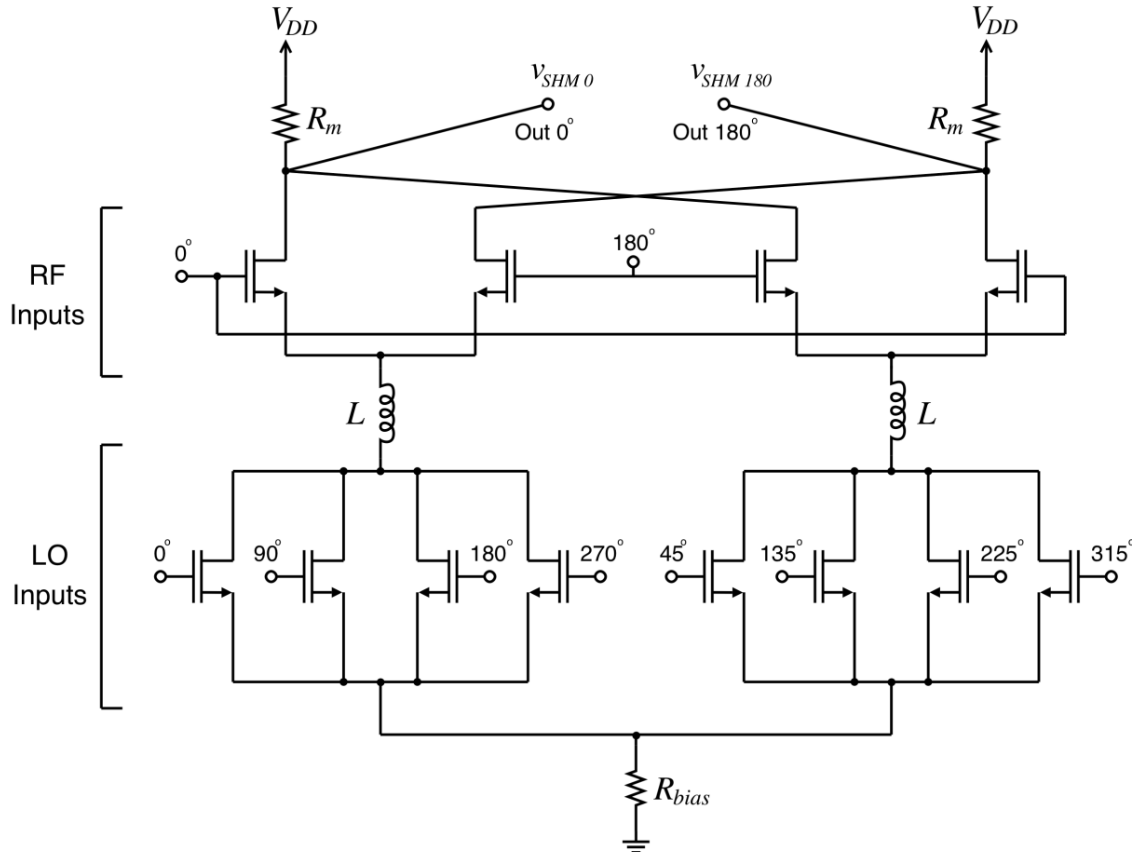
RF frequency	2.1 GHz
LO frequency	1 GHz
IF frequency	100 MHz
DC Power	36 mW
Chip Size	0.42 mm^2 incl. pads

mixer core (red box)

input/output active baluns (blue box)

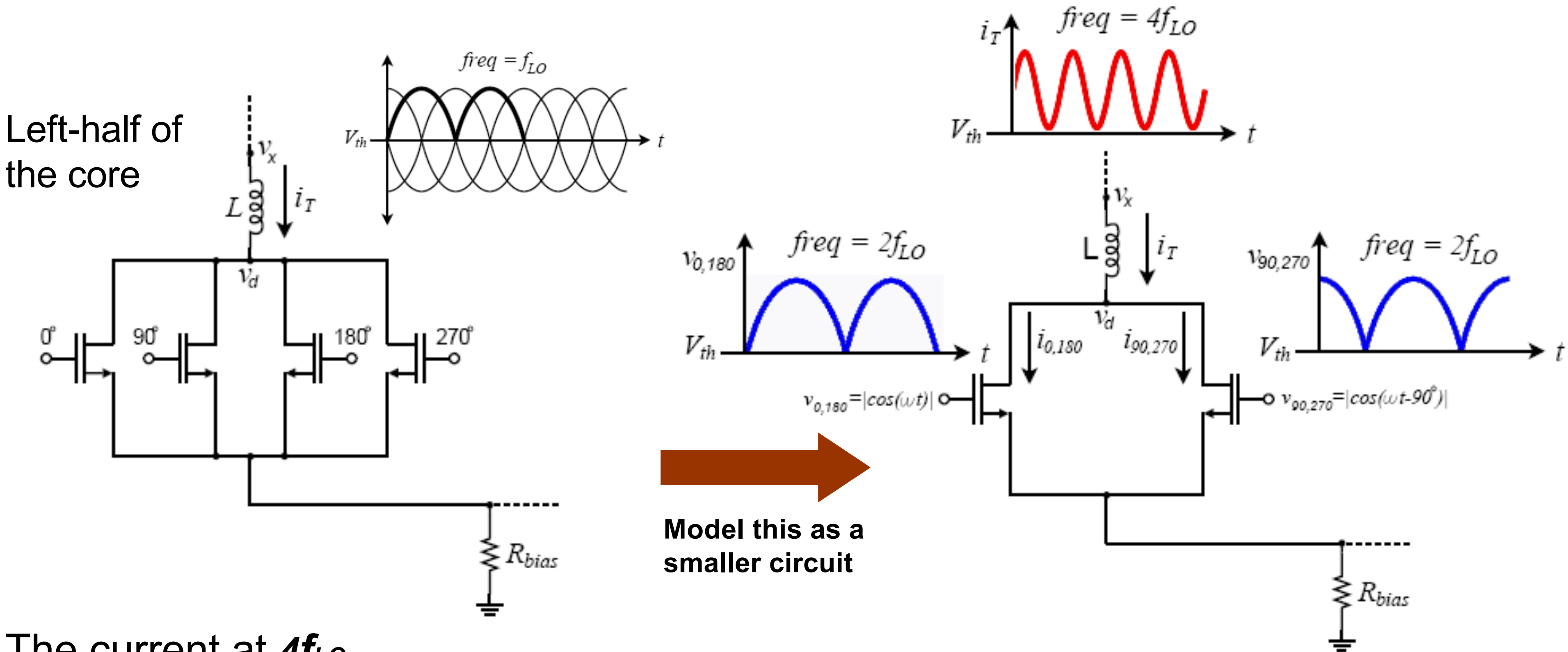
Recent Advances:

X4 Subharmonic Mixer



B. R. Jackson and C. E. Saavedra, "A CMOS Ku Band 4X Subharmonic Mixer," *IEEE Journal of Solid-State Circuits*, Vol. 43, No. 6, pp. 1351-1359, June 2008.

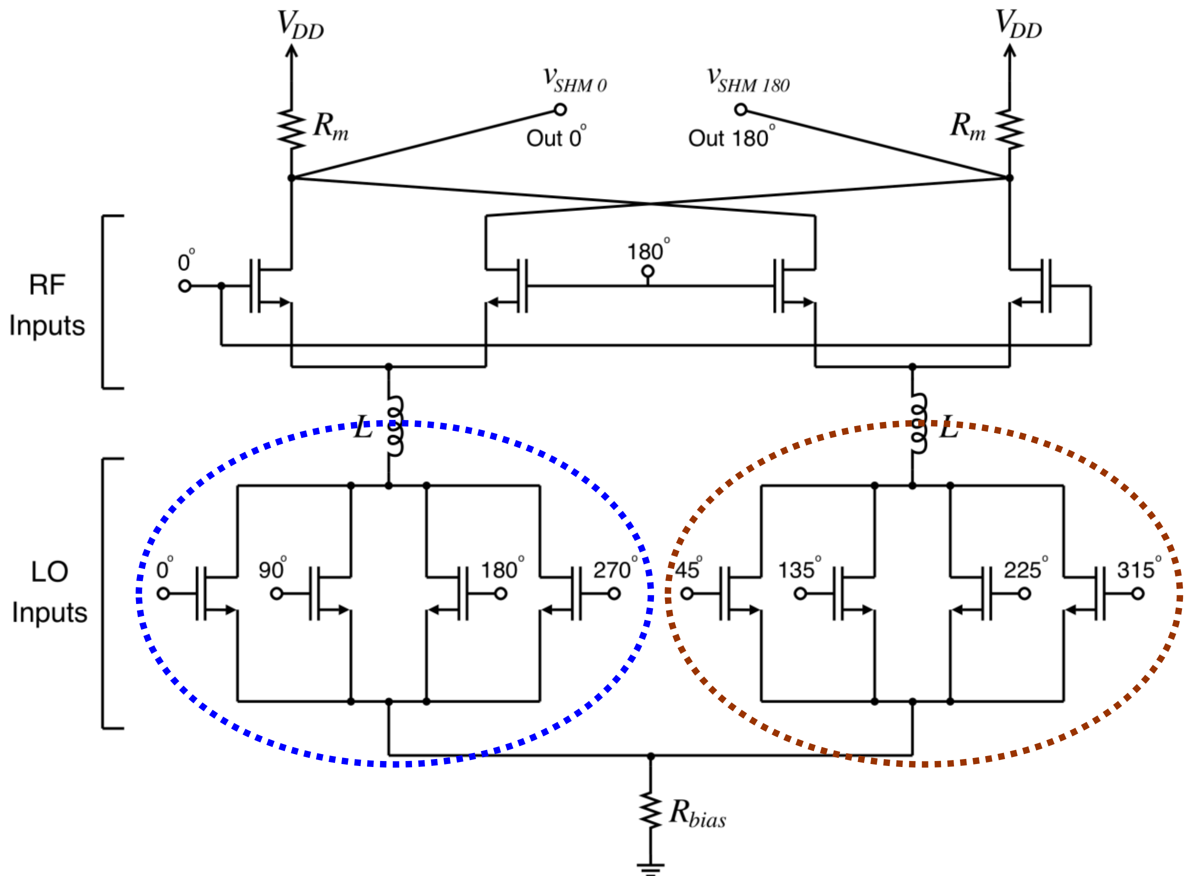
The LO Multiplication Core - modeling

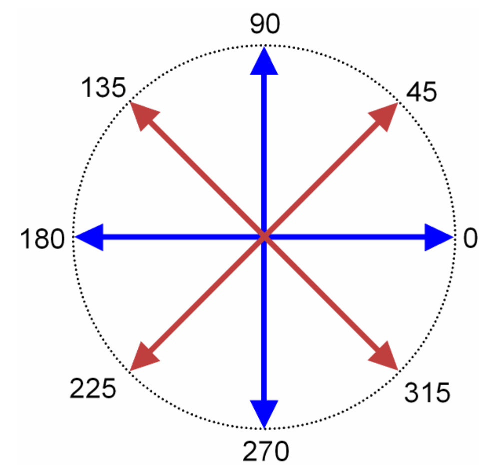


The current at ***4f***

$$i_T \approx \frac{1}{2}\mu_n C_{ox} W E_{sat} A_{LO}\left(\frac{15}{16}+\frac{1}{2}\left|\sin(2\omega_{LO}t)\right|+\frac{1}{16}\cos(4\omega_{LO}t)\right)$$

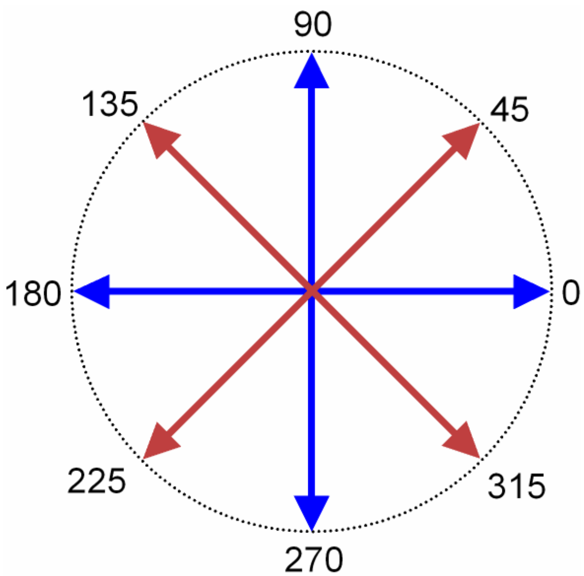
The LO phases in the multiplication core

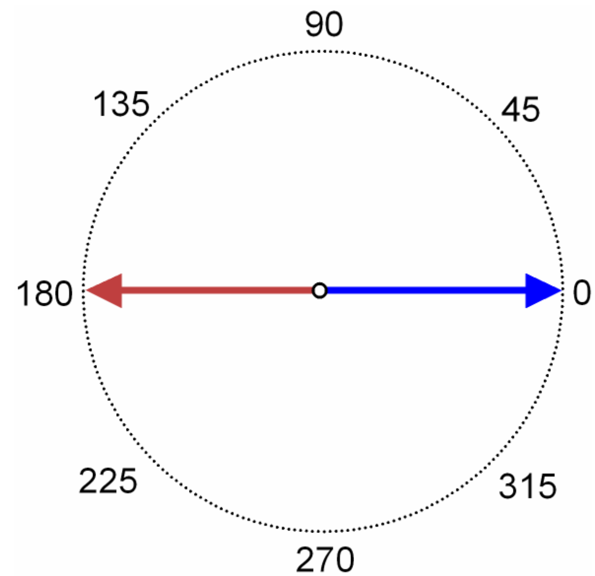




Octet-phase LO signal used to generate the ***4f****LO* signal

Creating a differential at signal at 4ωLO:





$$v_{LO}(t) = A_{LO}\sin\left(\omega_{LO}t + n\frac{2\pi}{8}\right) = A_{LO}\sin\left(\omega_{LO}t + n\frac{\pi}{4}\right)$$

n = 0, 1, 2, 3,…,7

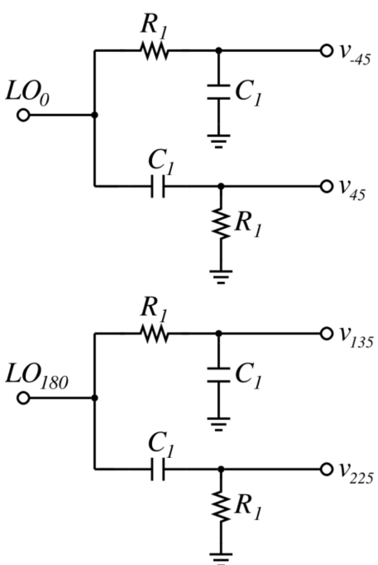
$$v_{4LO}(t) = v_d + i_T Z_{ind} \propto \sin\left(4\omega_{LO}t + n\pi\right)$$

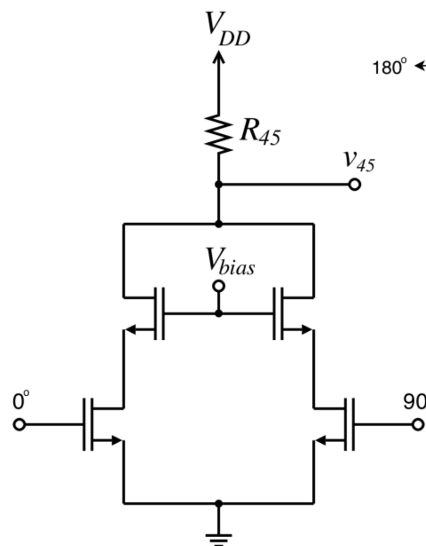
n = 0, 1, 2, 3,…,7

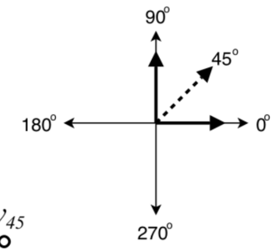
At the frequency, ω, the phases are: 0, π/4, π/2, 3π/4,…7π/4

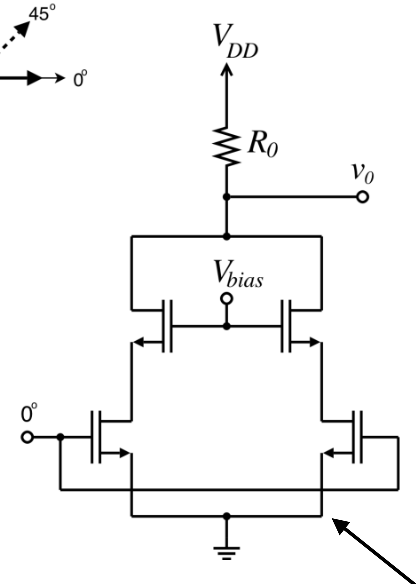
At the frequency, 4ω, the phases are: 0, π, 0, π,…

LO Octet Phase Generation







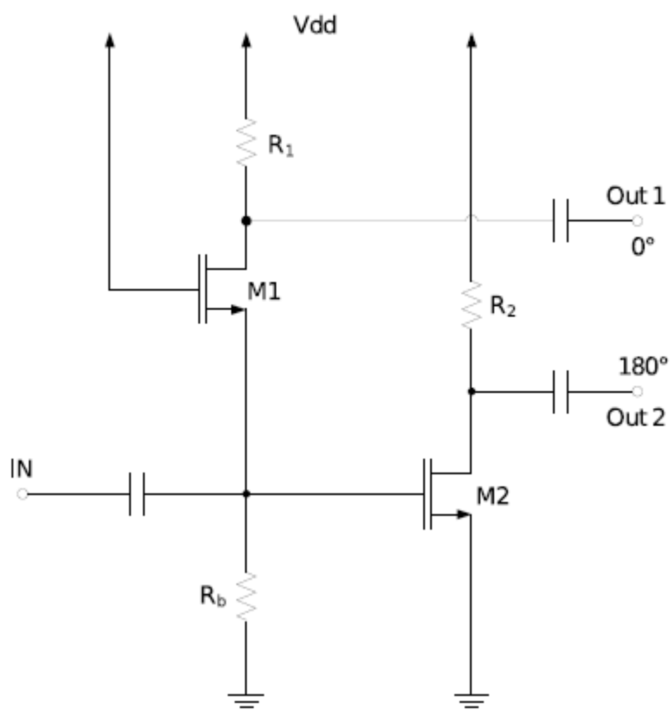


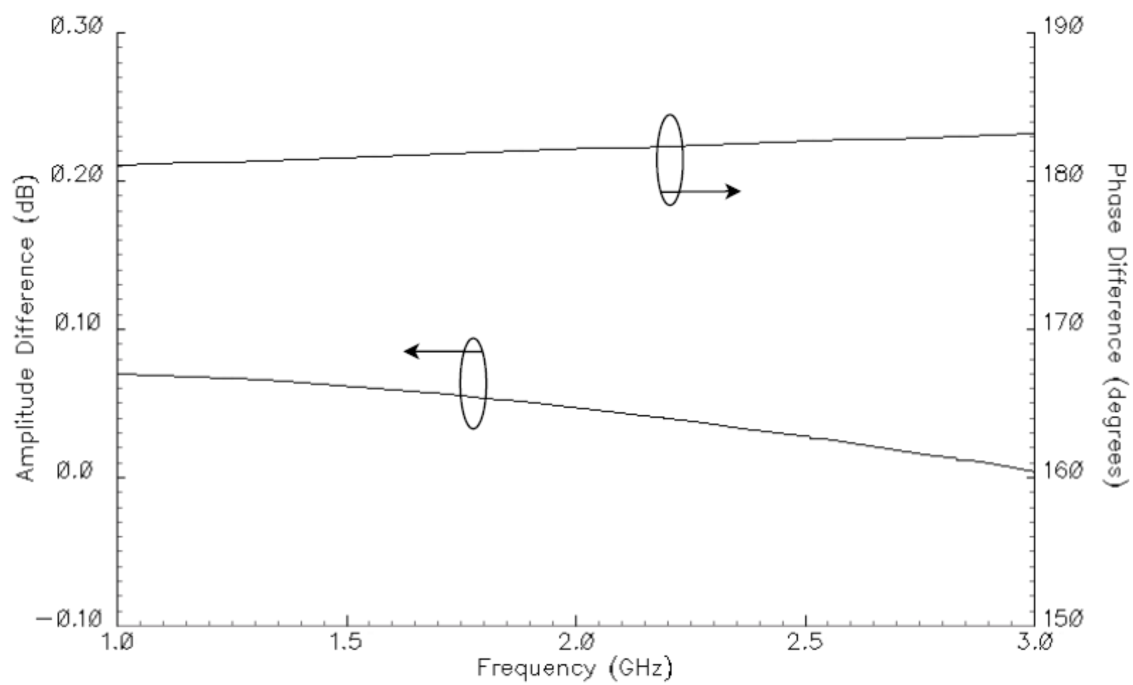
Create a set of quadrature signals using a method of your choice

Generate the π/4 vector: add a 0 and a π/2 vector using an active summing junction. Repeat for the other 3 vectors.

For equalizing the loading effects

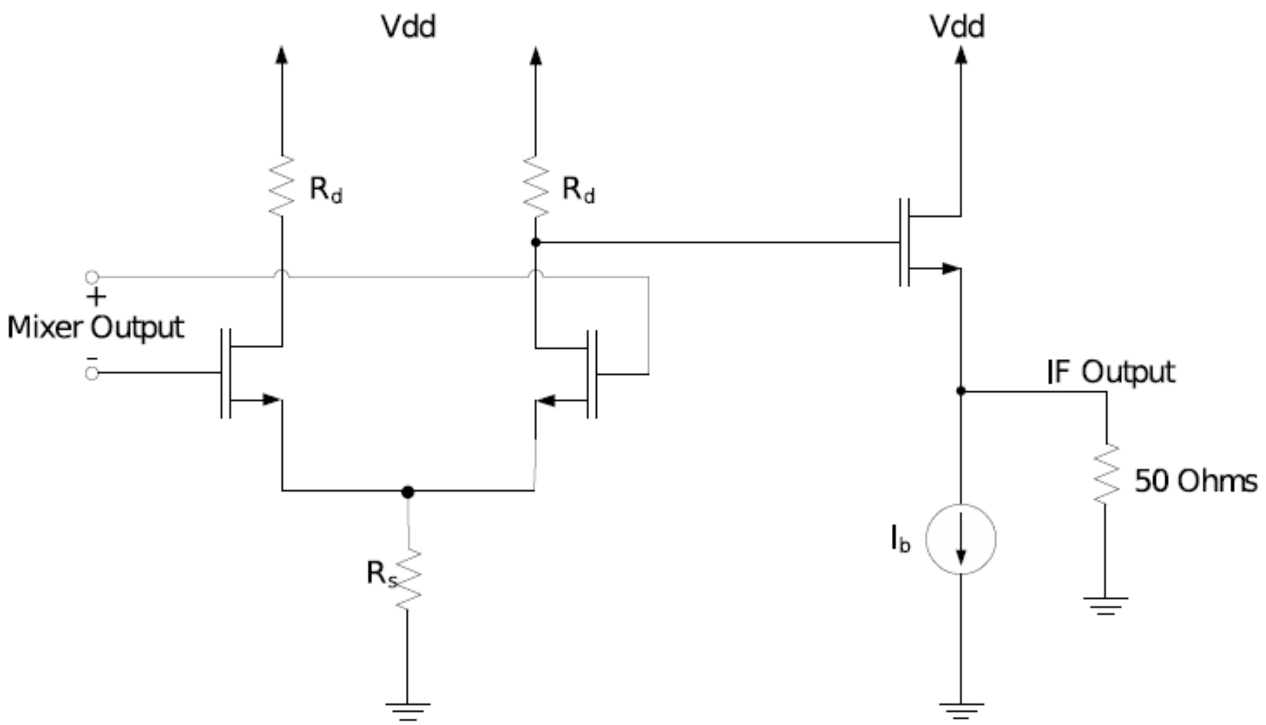
Fully integrated x4 SHP Mixer – I/O circuitry





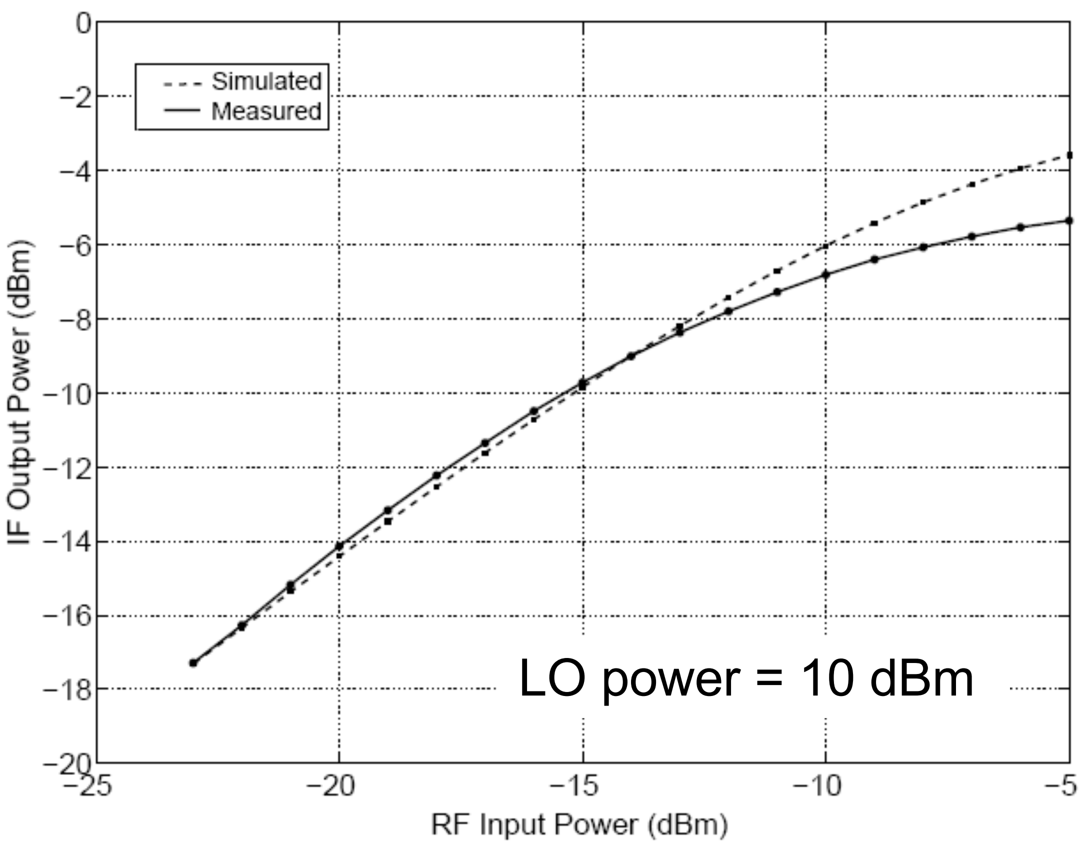
RF active balun

Fully integrated x4 SHP Mixer – I/O circuitry



IF output stage: differential to single-ended conversion

x4 SHM Power Performance

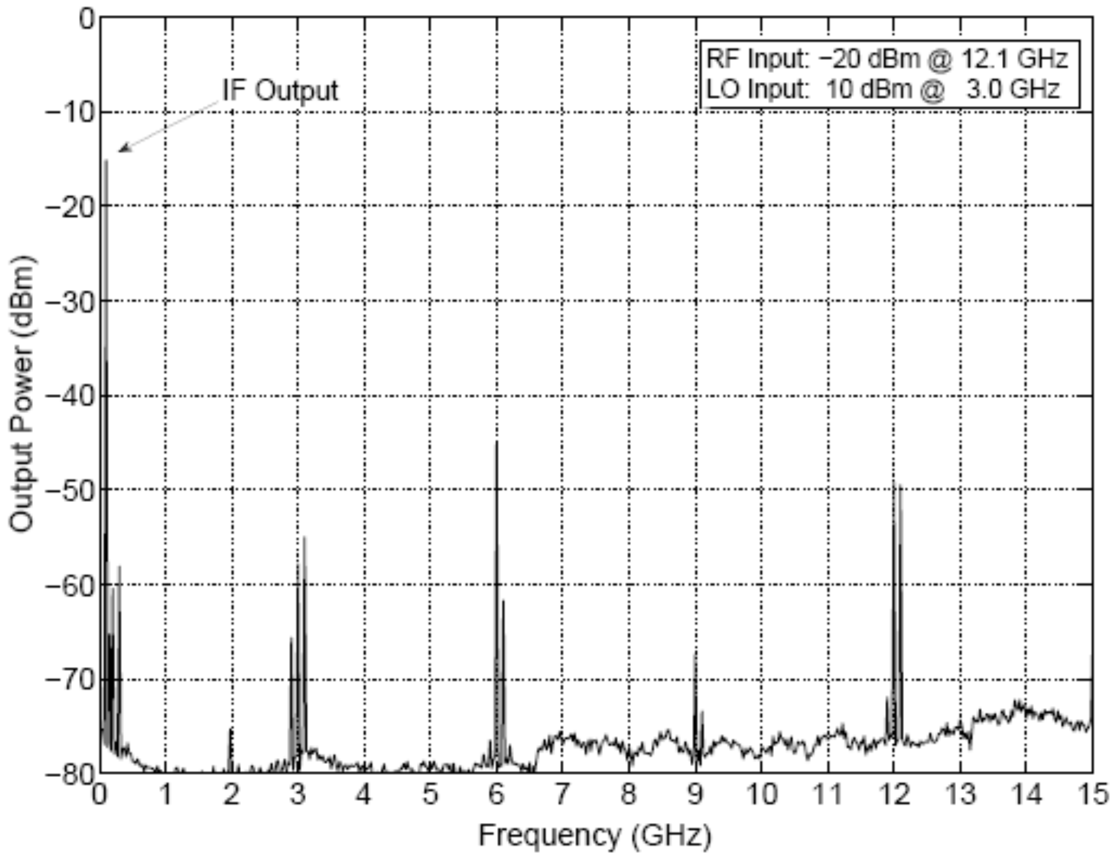


Conversion Gain: 6 dB
→ **best reported** to date for a x4 SHP mixer

$P_{1dB,out}$: -7 dBm

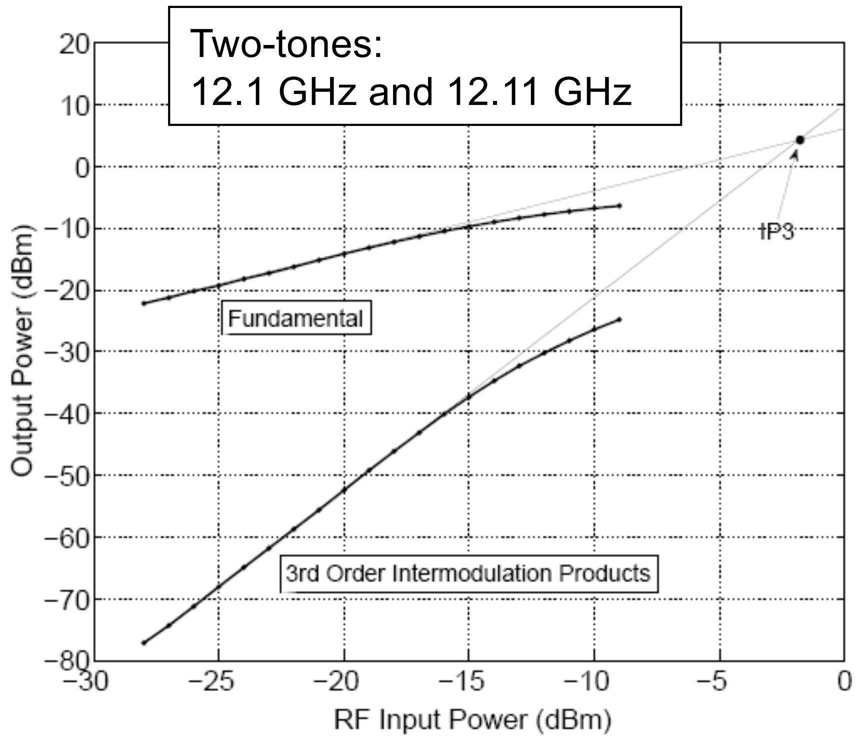
RF = 12.1 GHz, LO = 3.0 GHz, IF = 100 MHz

Spectral Response

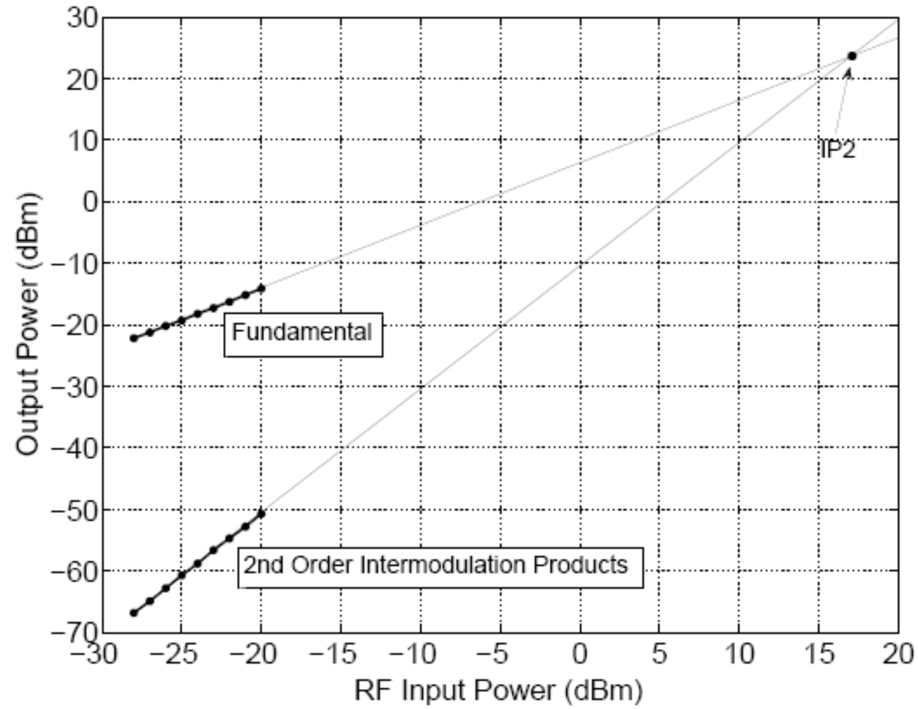


Ports	*Isolation*
RF–LO	43 dB
LO–RF	71 dB
2LO–RF	52 dB
4LO–RF	59 dB
RF–IF	30 dB
LO–IF	68 dB
2LO–IF	55 dB
4LO–IF	59 dB

Intermodulation Distortion Measurements



OIP3 = + 5 dBm



OIP2 = + 24 dBm

Using passive baluns will improve these values

LO Self-Mixing Performance

How to evaluate LO self-mixing behavior:

1) Measure the DC level at the IF port with no RF and LO input signals: V_{DC1}

2) Measure the DC level at the IF with an LO signal applied and no RF input signal: V_{DC2}

3) LO Self-Mixing is thus: $V_{Self-Mixing} = V_{DC1} - V_{DC2}$

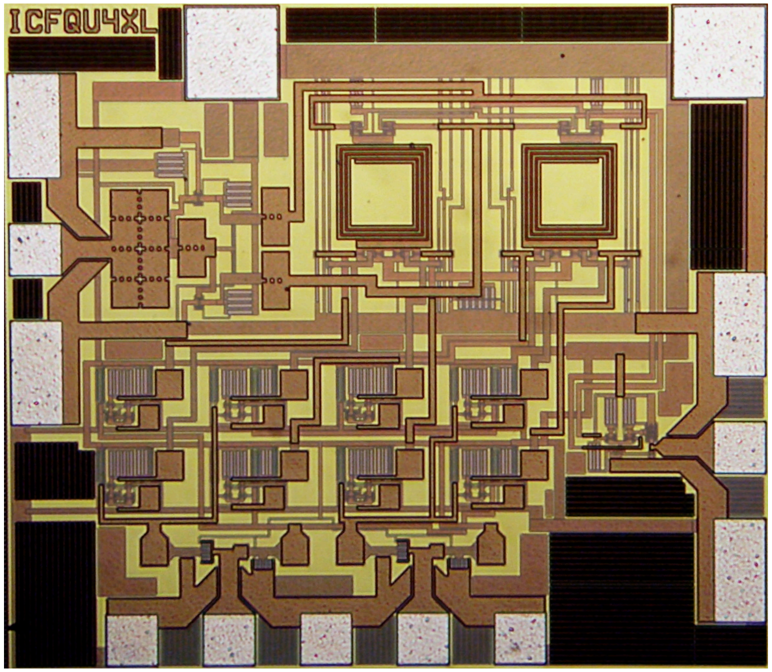
LO input signal used:

+10 dBm @ 3 GHz → V_{rms} = 707 mV

Measured self-mixing voltage at the IF port:

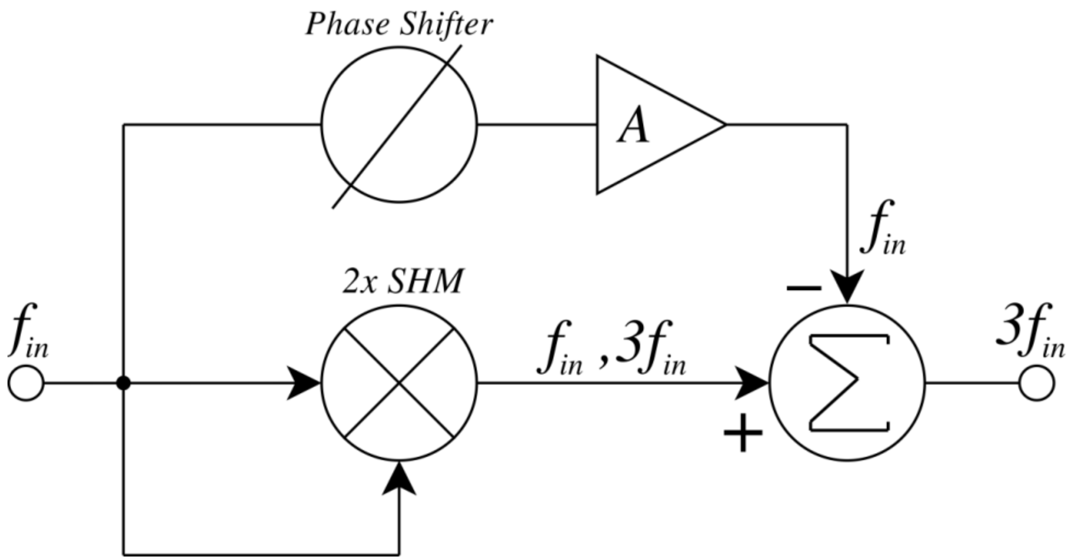
4.2 mV → 44 dB "rejection"

Ku Band x4 SHM Chip



RF frequency	12.1 GHz
LO frequency	3 GHz
IF frequency	100 MHz
Noise Figure	15 dB (DSB)
Chip Size	0.72 mm^2 incl. pads
DC Power	5 mW (mixer core)
	113 mW (full chip)

Frequency Multiplication with SHM's

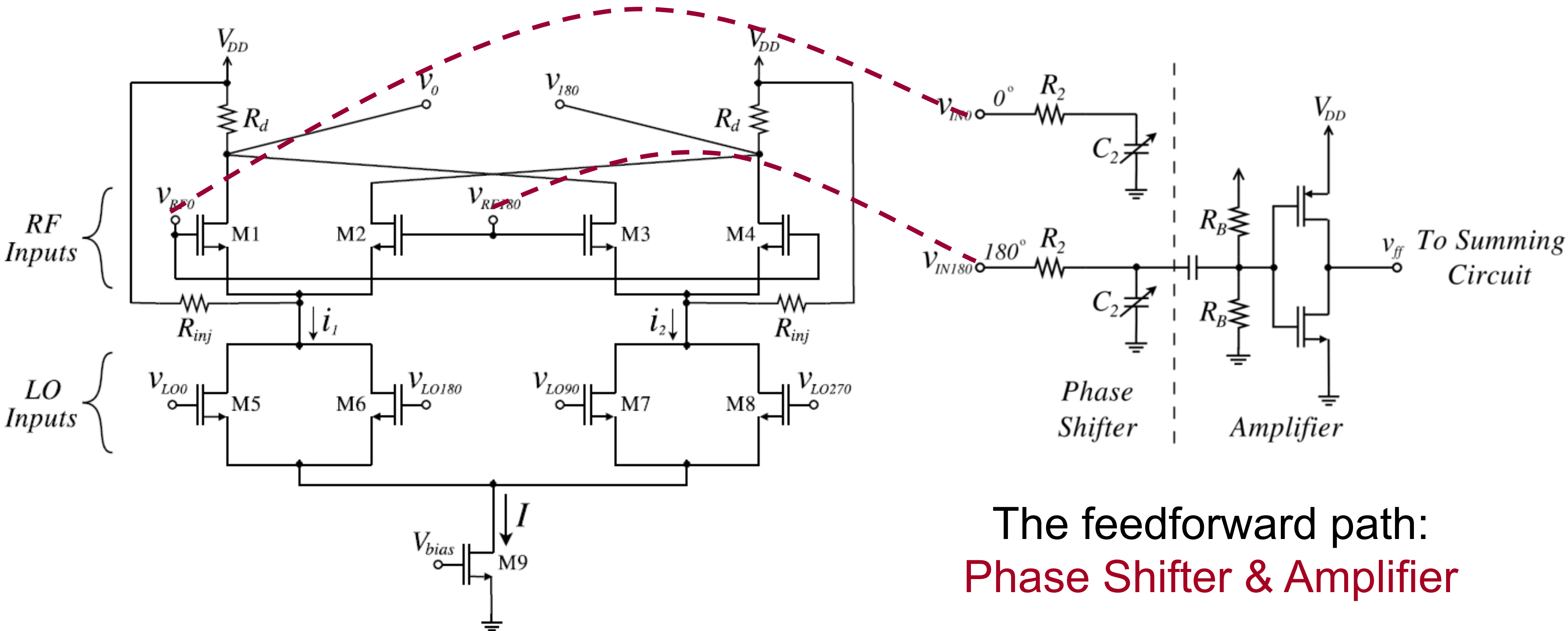


odd-order frequency multipliers can be conveniently designed

Frequency Tripler with Fundamental Signal Cancellation ⇨ No output filtering needed

B. R. Jackson, F. Mazzilli and C. E. Saavedra, "A Frequency Tripler using a Subharmonic Mixer and Fundamental Cancellation," *IEEE Transactions on Microwave Theory and Techniques,* Vol. 57, No. 5, pp. 1083-1090, May 2009.

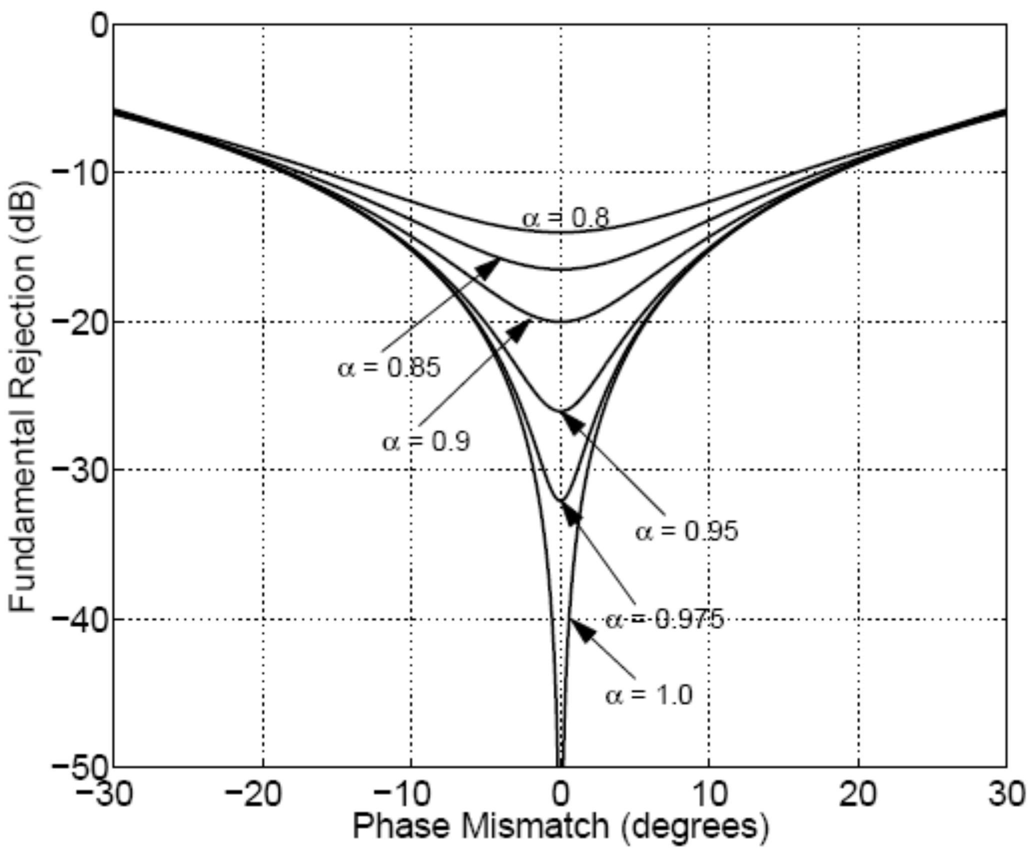
Frequency Tripler Design



The feedforward path:
Phase Shifter & Amplifier

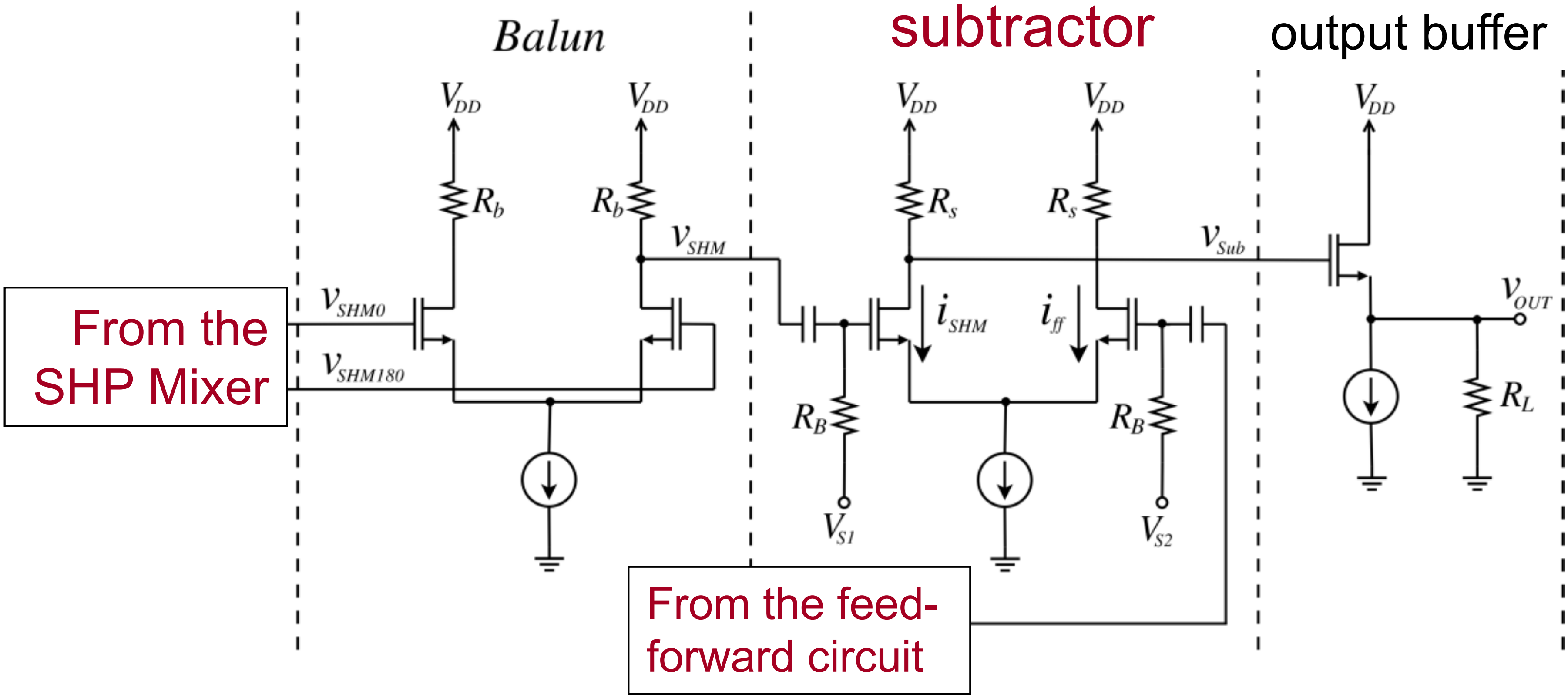
x2 Subharmonic Mixer

Effect of Phase and Amplitude Mismatch in the Fundamental Cancellation Process

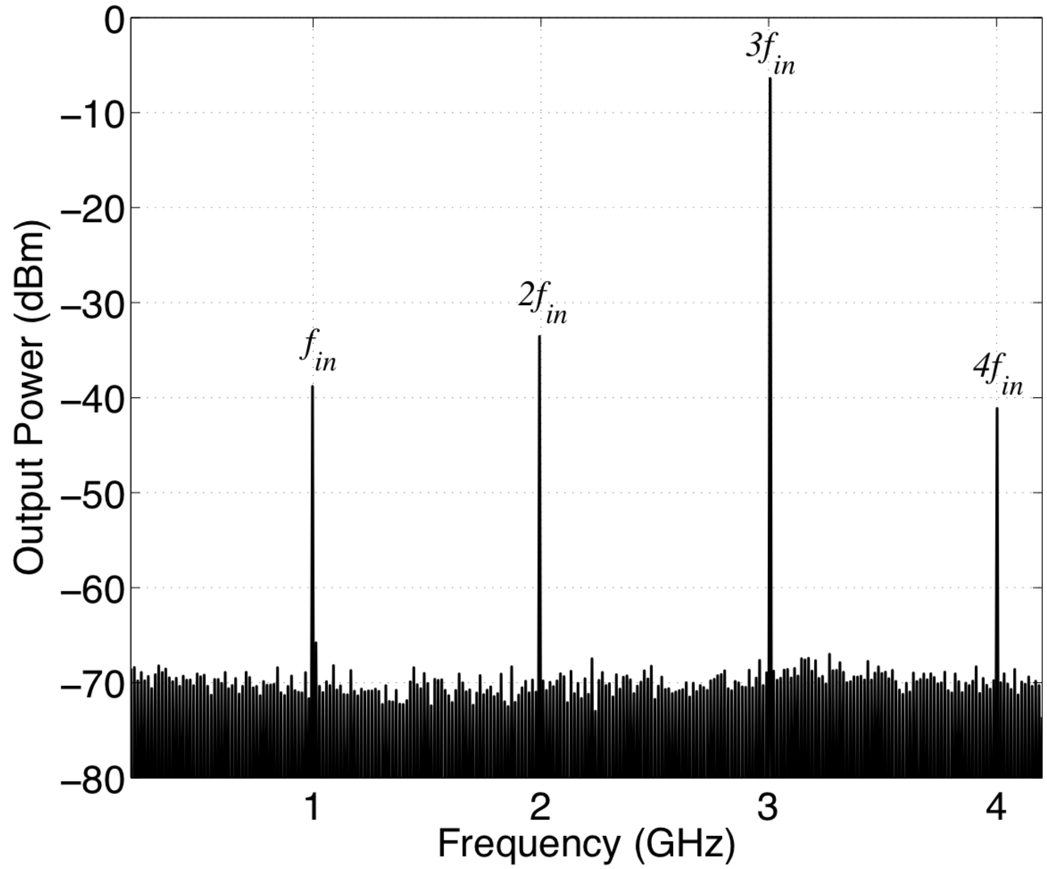


The **phase and amplitude** of the fundamental signal have to be **tuned for maximum** signal **cancellation** at the output.

Frequency Tripler Design – cont'd

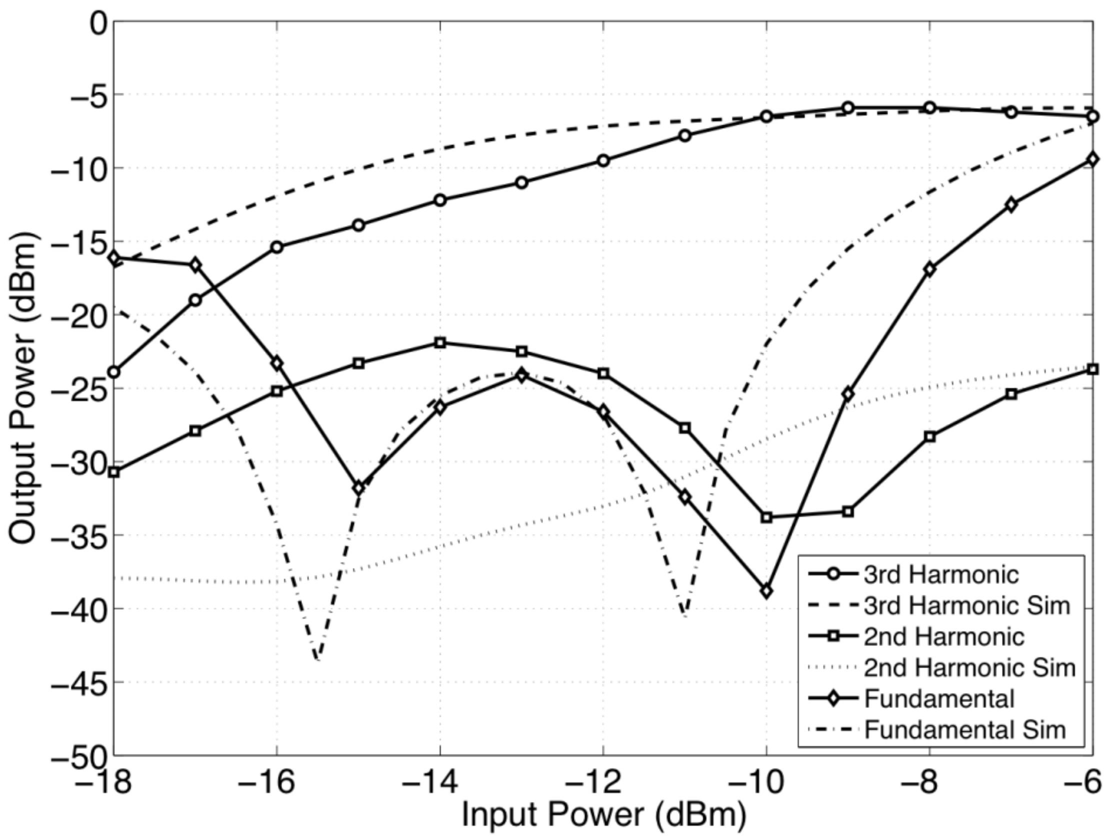


Output Spectrum



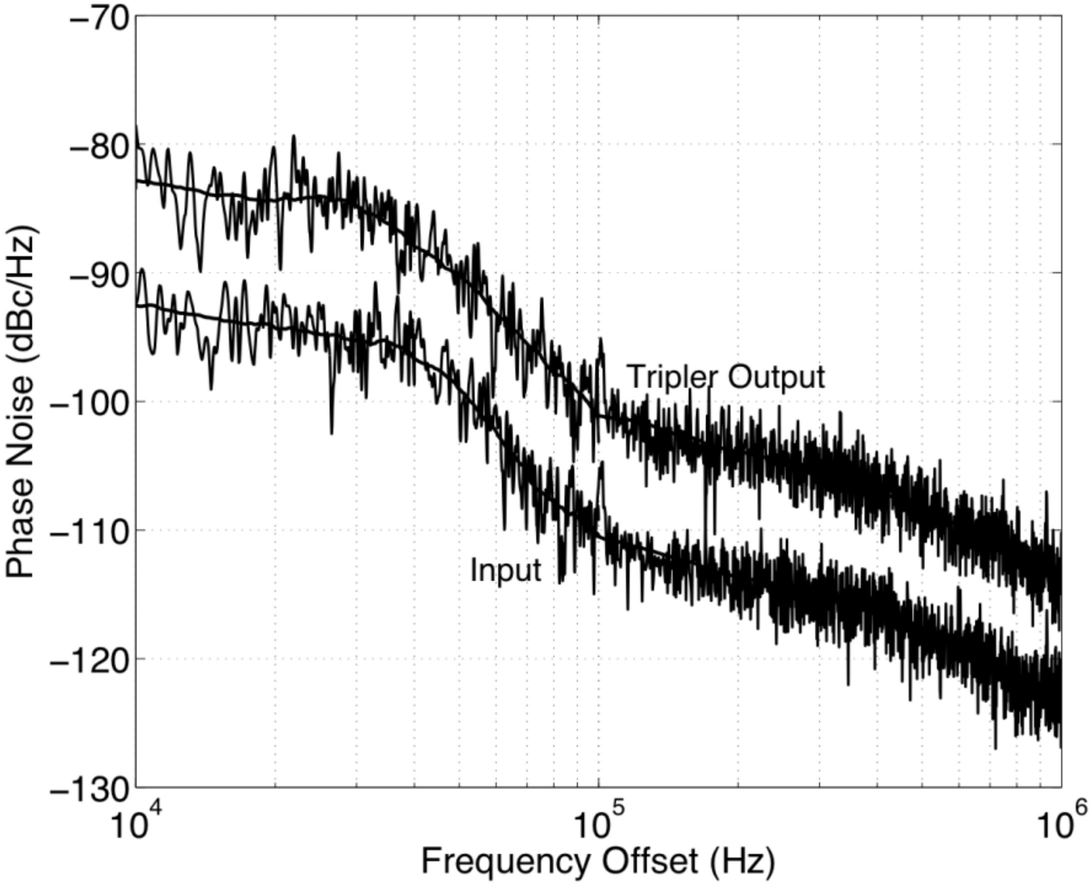
Input Freq.	1 GHz
Input power	-10 dBm
Output Freq.	3 GHz
Conv. Gain	3 dB
Fund. Reject.	30 dB

Power Performance



High suppression of the fundamental and other harmonics achieved without on-chip or off-chip filtering.

Noise Performance



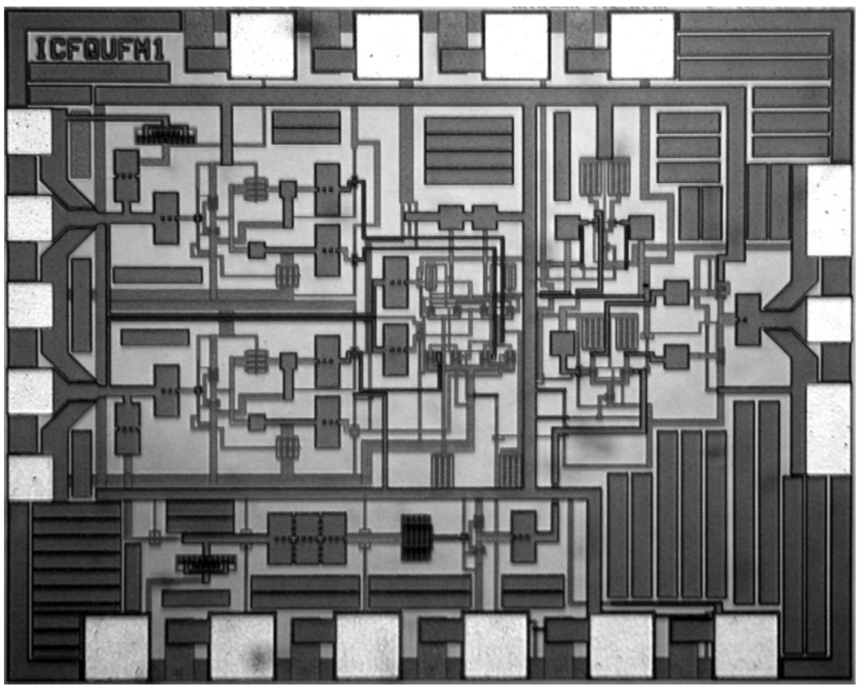
The minimum phase-noise degradation in a multiplier is:

$$20\log(n) = 9.54 \quad dB$$

for n = 3. In this work, the degradation is:

9.69 dB

Frequency Tripler Demonstration Chip



Input freq.	1 GHz
Output freq.	3 GHz
Fund. Reject.	30 dB
Chip Size	0.80 mm^2 incl. pads
DC Power	68 mW (full chip)

Conclusion

- In general, transistor-based SHM's can yield good levels of conv. gain: less than a fundamental Gilbert-Cell but higher than a diode SHM
- Excellent LO-to-RF and LO-to-IF isolation obtained due to the internal multiplication of the LO signal.
- By balancing gain and linearity requirements, the P_{1dB} and IP3 points can be optimized in a CMOS SHM
- Novel circuit concepts can be realized by using SHM's such as odd-order multipliers

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About the speaker:

Carlos Saavedra received the Ph.D. and M.Sc. degrees from Cornell University and the B.Sc. degree from the University of Virginia. From 1998-2000 he was with Millitech Corporation and in the year 2000 he joined Queen's University where he is now Associate Professor of Electrical and Computer Engineering and the Coordinator of Graduate Studies. Prof. Saavedra is a member of the Technical Program Committee of the IEEE RFIC Symposium and serves as a reviewer for several journals, including the IEEE T-MTT, IEEE MWCL, IEEE TCAS-II and Electronics Letters. He is a Senior Member of the IEEE.

http://post.queensu.ca/~saavedra/

References

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