Method to Improve the Conversion Gain Flatness of Transformer-Coupled Mixers

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***Abstract*— A 4-10 GHz, on-chip balun based current commutating mixer is proposed. Tunable resistive feedback is used at the transconductance stage for wideband response, and interlaced stacked transformer is adopted for good balance of the balun. Measurement results show that a conversion gain of 13.5 dB, an IIP3 of 4 dBm and a noise figure of 14 dB are achieved with 5.6 mW power consumption under 1.2 V supply. The simulated amplitude and phase imbalance is within 0.9 dB and $\pm 2^{\circ}$ over the band.**

***Index Terms*— Wideband mixer, on-chip balun, low power, current-commutating mixer.**

I. Introduction

A balun is desired to integrate into the double-balanced mixer, as most LNA designs reported are single-ended. One approach is to use an active balun such as the common gate-common source (CG-CS) balun in the transconductance stage of the mixer, as proposed in [1]. However, this method leads to higher power consumption. On the other hand, passive on-chip baluns have been extensively used due to its superior common mode rejection ratio (CMRR) while consuming no power [2], [3].

In the former transformer-coupled mixer designs, the transformer is usually operating in resonant mode [2], [4]. Although the high signal-to-noise ratio and current gain can be achieved in this way, the operation bandwidth is narrow. Thus, it is desired to design a transformer-coupled mixer that works in wide band.

This paper presents a low-power, wideband, on-chip balun based current commutating mixer with excellent performance. A tunable resistive feedback at the transconductance stage is used for achieving wideband response. A simple circuit model of the transformer is used in the frequency response analysis.

II. Mixer Design

As shown in Fig. 1, the proposed mixer is a folded current commutating mixer with its transconductance stage and the switching stage coupled by the balun T1. The transconductance stage is built with a single-ended cascode combined with a resistive feedback network. The switching stage is fully differential, so is the IF load, which is made of self-biased current source.

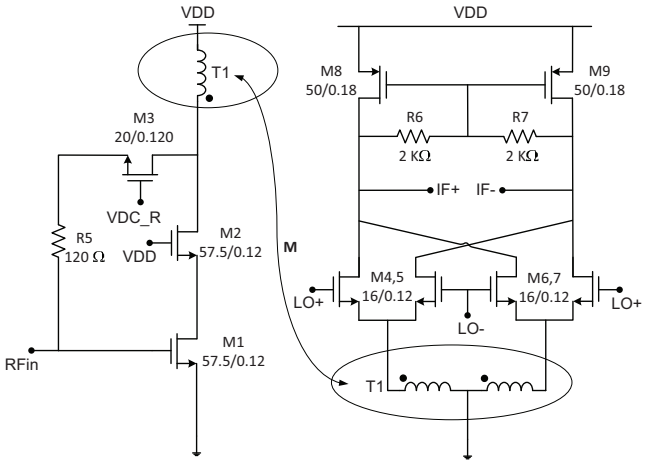

Fig. 1. Proposed broadband mixer configuration.

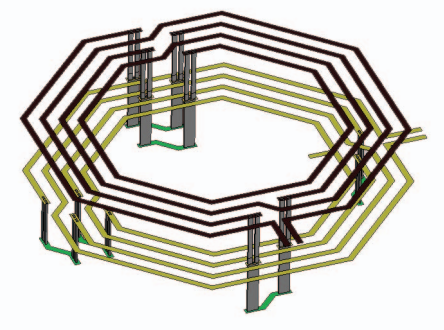

Fig. 2. Stacked monolithic balun configurations.

The balun is implemented fully on chip in a standard CMOS 1P8M process. As shown in Fig. 2, stacked structure is adopted for high coupling factor, i.e. the primary spiral is built in the top metal layer and secondary spiral in the second from the top layer. Fig. 3 demonstrates both the top view and the side view of the balun. As can be observed, the primary and the secondary spirals are both octagonal and center-tapped symmetric, and the primary and secondary windings are interlacing to decrease the overlapping capacitance between the spirals. The turns

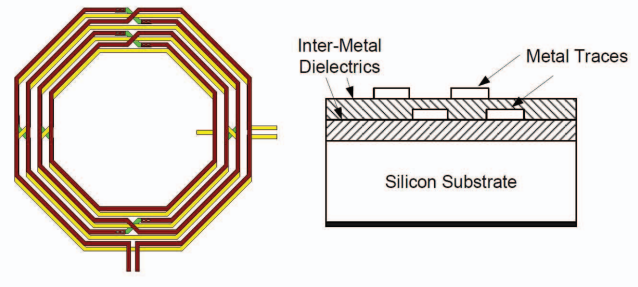

Fig. 3. Top and side views of the balun

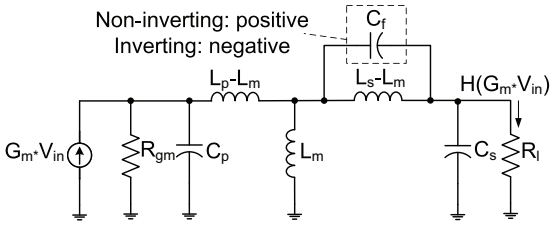

Fig. 4. Simplified balun circuit model of one branch.

ratio is 4:2:2, and the diameters of the spirals are 170 μm.

The conversion gain of the current commutating mixer can be generalized as

$$A_{V,mixer} = \frac{2}{\pi} g_m H(j\omega) Z_L \tag{1}$$

$H(j\omega)$ stands for the portion of the RF current fed into the switching stage, and it determines the frequency response of the conversion gain. In this work, a wideband response of $H(j\omega)$ is obtained through elaborately designing the network around the transformer.

Since the balun is fully symmetric, the same equivalent circuit configurations are chosen for the noninverting and inverting branches without losing accuracy. The equivalent circuit is depicted in Fig. 4. In this circuit, L_m represents the mutual inductance between the spirals while $L_p - L_m$ and $L_s - L_m$ represent the leakage inductance of each side, respectively. C_p and C_s represent the capacitance at primary and secondary terminals. A Norton equivalent circuit is used to represent the transconductance stage, and R_l represent the input impedance of the switches. C_f models the effect of the parasitic capacitors between the two spirals. All the component values are identical for the circuits of noninverting and inverting branches, except that C_f is positive in the non-inverting branch and negative in the inverting one.

In circuit, $H(j\omega)$ of (1) is the transfer function from current source $G_m * V_{in}$ to the current going through R_l. In the following transfer function analysis, the effect of C_f is ignored and will be discussed later when imbalance of the balun is addressed.

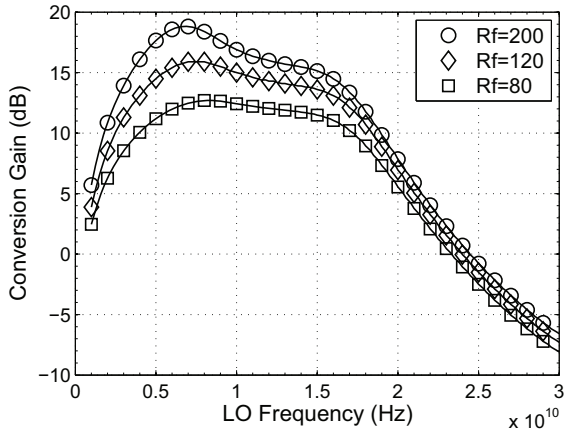

Fig. 5. Simulated frequency response with different R_f.

TABLE I
SPECIFICATIONS WITH DIFFERENT FEEDBACK RESISTORS

R_f (ohms)	200	**120**	80
Noise Figure (dB)	9.6	**13.3**	15.0
OIP3 (dBm)	15.5	**18.3**	20.5

The circuit in Fig. 4 are two resonators (L_p, C_p) and (L_s, C_s) coupled by L_m. There are two peaks in the response, and it's the detach of the two peaks that forms the wide passband. The position of the two peaks are given in (2) [5].

$$\omega_{1,2} = \sqrt{\frac{(L_pC_p + L_sC_s) \pm \sqrt{(L_pC_p - L_sC_s)^2 + 4C_pC_sL_m^2}}{2(L_pL_sC_pC_s - C_pC_sL_m^2)}} \tag{2}$$

Through properly choosing R_{gm} and R_l, the Q of the resonators are small so that a flat response over the passband can be achieved. In the mixer design, R_l is determined by the switch transistor size, and R_{gm} can be tuned by the feedback resistor R_f. In this work, NMOS of $16\mu m/0.12\mu m$ is used for the switch. With an LO power of -5 dBm and the IF frequency kept at 110 MHz, the frequency response of the mixer is simulated with different R_f, as shown in Fig. 5. As can be observed, proper switch size is chosen so that the second peak located around 15 GHz is moderate. With the increase of the feedback resistor, the first peak is flattened, and up to 12 GHz bandwidth can be achieved. Meanwhile, the peak gain drops because the effective transconductance decreases with the increase of R_f.

The feedback resistance affects other performances of the mixer, too. The OIP3 and noise figure at the peak frequency with different feedback resistors are given in Table I. The variation tendency of OIP3 and the noise figure accords to the prediction, as the feedback decreases the effective transconductance while suppresses the distortion of the input transistor. In this work, R_f of 120 ohms is

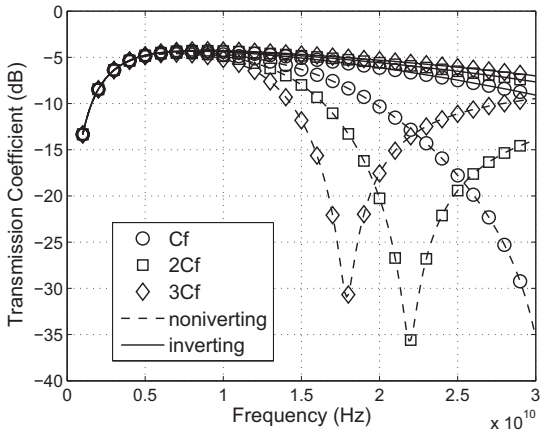

Fig. 6. Magnitude response of the balun's circuit model with different C_f.

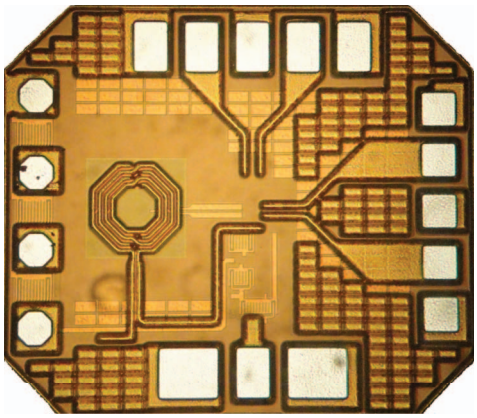

Fig. 7. The microphotograph of the chip.

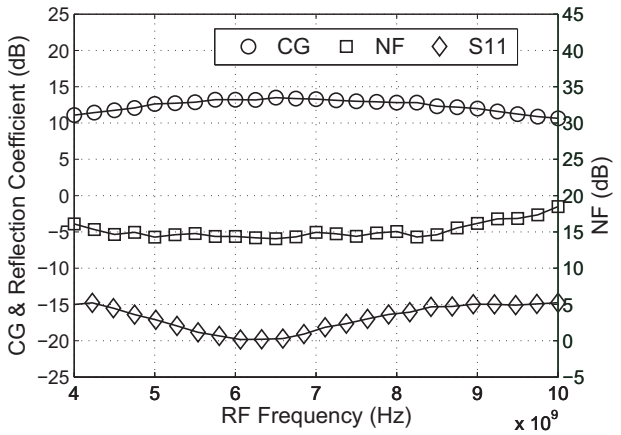

Fig. 8. Conversion gain, reflection coefficient and noise figure.

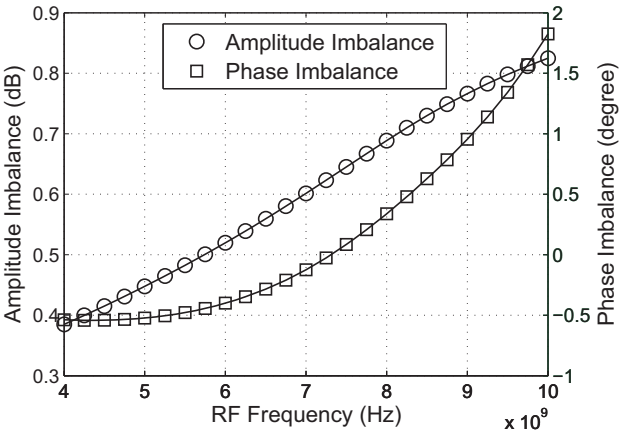

Fig. 9. Simulated amplitude and phase imbalance.

chosen to trade some bandwidth for lower noise figure. As shown in Fig. 5, although the passband of 4 GHz to 10 GHz is around the first peak, the existence of the second peak prevents the response from rolling off drastically.

The balance of the balun is another important specification. For a multifilament-transformer-based balun, imbalances can originate from the parasitic capacitor between the two overlapping spirals [6], which manifests itself as C_f in the circuit model in Fig. 4. Due to the sign of the transfer ratio, C_f is positive in the noninverting branch and negative in the inverting one. The positive C_f adds a notch in the frequency response of noninverting branch, which is absent in its inverting counterpart. In this manner, the frequency responses for the two branches are different from each other, and imbalance is generated even though the spirals are symmetric.

To verify this behavior, the transmission coefficient of the equivalent circuit extracted from the balun are simulated, as shown in Fig. 6. In the simulation, extra C_f is added to the circuit to manifest its influence to the frequency response. As can be observed, with the increase of C_f, the notch frequency of the noninverting branch decreases while the response of inverting branch does not change much. Consequently, the balance between the two branches tend to deteriorate. Thus, in order to improve the balance, the stacked spirals are designed to interlace with one another for the least overlapping, as can be observed from both Fig. 2 and Fig. 3.

III. Measurement Results

The mixer is fabricated in IBM's CMOS 130μm technology and a photograph of the IC is shown in Fig. 7. It occupies a die area of 800×920 μm^2. The circuit consumes only 5.6 mW of dc power from a 1.2 V voltage supply.

The mixer IC is measured directly on-wafer using 40 GHz coplanar waveguide (CPW) probes and dc probes. A 45 GHz Keysight spectrum analyzer (E4446A) with the NF measurement personality software is used for gain, NF and linearity measurements, and a 50 GHz Keysight network analyzer (8510C) is used for input reflection coefficient measurement. At the LO input, an external 180° hybrid is necessary to provide differential signals from the single-

ended source. And at the IF output, an off-chip differential-to-single-ended buffer with a high input impedance and unity voltage-gain is employed, too, for the convenience of measurements.

Fig. 8 shows the measured conversion gain, DSB NF and the reflection coefficient versus RF frequency. In these measurements, the LO frequency is swept in tandem with the RF frequency, keeping the IF frequency fixed at 110 MHz, and the LO power is fixed at -5 dBm. As can be observed, the conversion gain reaches its peak of 13.5 dB at 6.5 GHz, and is 11.1 dB and 10.6 dB at 4 GHz and 10 GHz, respectively, ensuring the gain drop less than 3 dB across the band. The DSB NF curve has a reciprocal shape compared to the conversion gain curve, i.e. at the frequency where the peak gain is achieved, the NF reaches the minimum value, while at two edges of the band where conversion gain is lower, higher NF is obtained. The minimum NF achieved is 14.06 dB at 6.5 GHz. Due to the resistive feedback at the transconductance stage, the mixer also provides a good input matching to 50 ohms. VNA measurement result shows that S11 of the chip is below -13 dB across the entire frequency range.

Both IIP3 and P1dB are measured to evaluate the linearity performance of the mixer. The IIP3 is 3.98 dBm and input referred P1dB is -7.96 dBm. The good linearity performance results from two aspects of the mixer configuration. One is the large voltage headroom at mixer output due to the folded structure, and the other one is the distortion suppression of the resistive feedback in the transconductance stage. In addition, simulation results in Fig. 9 show that the amplitude and the phase imbalance is within 0.9 dB and $\pm 2^\circ$, respectively, from 4 GHz to 10 GHz. The performance of this work is compared with other mixers with on-chip balun in Table II.

TABLE II
PERFORMANCE COMPARISON

Reference	this work	[7]	[1]	[8]
Process	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS	2μm GaInp/GaAs
Freq. (GHz)	4$\sim$10	0.5$\sim$5.7	2$\sim$11	1.5$\sim$14
CG (dB)	13.5	5.44$\sim$17.05	8.4	20
IIP3 (dBm)	4	-9.95$\sim$5.83	6.5	-3
DSB NF (dB)	14.06	13.4$\sim$21.9	12.5	23
Pdis. (mW)	5.6	6.2	25.7	43.5
Amp. Imbal.*(dB)	0.9	2	15	-
Phase Imbal.*($^\circ$)	$\pm 2^\circ$	3°	4°	-

* The amplitude and phase imbalances are simulation results.

IV. CONCLUSION

This paper presents a low-power, wideband, on-chip balun based current commutating mixer. A tunable resistive feedback is used at the transconductance stage for wideband frequency response and input matching. The measurement results show that 13.5 dB conversion gain is achieved, with a high IIP3 of 4 dBm and noise figure of 14 dB. The amplitude and phase imbalance is within 0.9 dB and $\pm 2^\circ$.

REFERENCES

[1] P.-Z. Rao, T.-Y. Chang, C.-P. Liang, and S.-J. Chung, "An ultra-wideband high-linearity CMOS mixer with new wideband active baluns," *IEEE Trans. Microwave Theory Tech.*, vol. 57, no. 9, pp. 2184–2192, Sept 2009.

[2] J. Long and M. Copeland, "A 1.9 GHz low-voltage silicon bipolar receiver front-end for wireless personal communications systems," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1438–1448, Dec 1995.

[3] R.-F. Ye, T.-S. Horng, and J.-M. Wu, "Low-noise and high-linearity wideband CMOS receiver front-end stacked with glass integrated passive devices," *IEEE Trans. Microwave Theory Tech.*, vol. 62, no. 5, pp. 1229–1238, May 2014.

[4] C. Hermann, M. Tiebout, and H. Klar, "A 0.6-V 1.6-mW transformer-based 2.5-GHz downconversion mixer with +5.4-dB gain and -2.8-dBm IIP3 in 0.13- μm CMOS," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 2, pp. 488–495, Feb 2005.

[5] J. Hong, "Couplings of asynchronously tuned coupled microwave resonators," *IEE Peoc. Microwaves, Antennas and Propag.*, vol. 147, no. 5, pp. 354–358, Oct 2000.

[6] J. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sept 2000.

[7] X. Zhang, X. Cui, B. Wang, and C. L. Lee, "A UWB mixer with a balanced wide band active balun using crossing centertaped inductor," in *IEEE Int. Symp. Circuit Syst.*, May 2013, pp. 1588–1591.

[8] S.-C. Tseng, C. Meng, and C.-K. Wu, "GaInp/GaAs HBT wideband transformer Gilbert downconverter with low voltage supply," *Electron. Lett.*, vol. 44, no. 2, pp. 127–128, January 2008.