A +18 dBm Broadband CMOS Power Amplifier RFIC with Distortion Cancellation

Ahmed M. El-Gabaly[1,2] and Carlos E. Saavedra[1]

[1]Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada K7L 3N6
[2]Peraso Technologies Inc., Toronto, ON, Canada M5J 2L7

***Abstract*— A broadband fully-integrated class-A power amplifier (PA) is presented using derivative superposition (DS), which delivers +18 dBm of saturated output power from 1 GHz to 6 GHz. The PA exhibits a flat power gain of 13.5 ± 1.2 dB over its operating frequency range. It features a high linearity with an output 1dB compression point ($\mathrm{OP_{1dB}}$) and third order intercept point (OIP3) of more than +16 dBm and +25 dBm respectively. The measured OIP3 remains above +25 dBm, i.e. 9 dB higher than $\mathrm{OP_{1dB}}$, for a wide range of power levels up to 4 dB backoff from $\mathrm{OP_{1dB}}$. The chip was fabricated using a 0.13μm CMOS process, occupying an active area of only 200μm×110μm.**

***Index Terms*— Distortion cancellation, derivative superposition, power amplifiers, CMOS, RFIC**

I. Introduction

Much of the research and development on microwave power amplifiers (PAs) is rightly focused on simultaneously maximizing their linearity and power efficiency because of the multitude of battery-operated wireless devices in our daily lives that are connected to Wi-Fi and WPAN networks. Examples of linearization techniques for amplifiers include predistortion [1]–[3], feedforward [4]–[6], derivative superposition (DS) [7]–[10], plus a few others.

Co-existing with the hand-held mobile devices there are a nontrivial number of other devices for the wireless infrastructure that draw their power from the grid. Infrastructure-related, 'non-mobile', devices include home/office routers and Wi-Fi enabled desktop computers, printers, scanners and more. As the complexity of communications standards increase in order to handle more users and data, the linearity and bandwidth specifications of RF PAs are becoming more stringent. Class A or AB PAs offer high linearity and broadband performance for grid-operated devices in comparison to switched-mode PAs (e.g. Class E or F) that are well suited for high efficiency in battery-operated mobile devices [11].

This paper describes the design and measurement of a broadband fully-integrated CMOS class-A PA with cascode transconductors that can deliver up to +18 dBm of saturated output power ($\mathrm{P_{SAT}}$) over a wide frequency range from 1 GHz to 6 GHz. The PA exhibits a flat power gain of 13.5 ± 1.2 dB, an output 1dB compression point ($\mathrm{OP_{1dB}}$) of +16.3 dBm, an output third-order intercept point (OIP3) of +25.6 dBm and a power-added efficiency (PAE) of 44.3% over its operating frequency range. DS is used to reduce the distortion produced by the PA in a manner that does not require bias adjustments for different frequencies and power levels. The RF integrated circuit (RFIC) was fabricated using a 0.13-μm CMOS process and has a small active area of only 200μm×110μm.

II. CMOS PA Circuit Description

A circuit schematic of the low-distortion CMOS PA is shown in Fig. 1 and is based on the approach used for the gallium-nitride PA described in [10]. Transistors $\mathrm{M_1}$ and $\mathrm{M_2}$ constitute the main signal path of the amplifier, whereas transistors $\mathrm{M_{1A}}$ and $\mathrm{M_{2A}}$ form the auxiliary path. $\mathrm{M_1}$ is biased in saturation and its drain-to-source current can be written using the power series

$$i_{DS} = I_{DS} + g_{m1}v_{GS} + g_{m2}v_{GS}^2 + g_{m3}v_{GS}^3 + ... \quad (1)$$

where I_{DS} is the bias or quiescent drain-source current, v_{GS} is the gate-source voltage and

$$g_{mn} = \frac{1}{n!}\frac{\partial^n i_{DS}}{\partial v_{GS}^n}. \quad (2)$$

For strong inversion and class A operation, $\mathrm{M_1}$ has a negative g_{m3} coefficient. $\mathrm{M_{1A}}$ is biased near pinch-off such

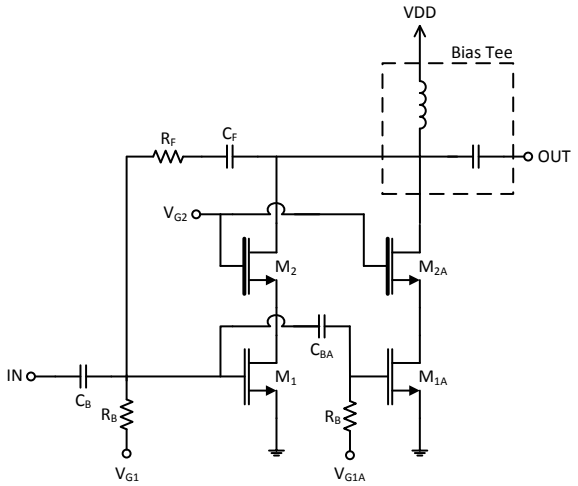

Fig. 1. Circuit schematic of the CMOS PA.

TABLE I
SUMMARY OF COMPONENT VALUES FOR THE PA

Transistor	$(W/L)_1$	$(W/L)_2$	$(W/L)_{1A}$	$(W/L)_{2A}$	
Size (μm)	200/0.12	300/0.4	75/0.12	135/0.4	
Component	R_B	C_B	C_{BA}	R_F	C_F
Values	10 kΩ	5 pF	2 pF	340 Ω	1.2 pF

that its g_{m3} term is positive. In this manner, the third-order intermodulation distortion (IMD3) tones produced in the main path and the auxiliary path will have opposite phases and will cancel when they are combined at the output. The gate width and bias voltage of $\mathrm{M_{1A}}$ are chosen such that the IMD3 tones generated in the auxiliary path have approximately the same magnitude as those in the main path for good cancellation. Since the auxiliary path operates near pinch-off, its dc power consumption is small compared to the main one. As a result, this distortion-cancelling topology only has a minor effect on the amplifier's power efficiency.

The second-order nonlinear current of $\mathrm{M_1}$, $g_{m2}v_{GS}^2$ in (1), can feed back to the gate and source of $\mathrm{M_1}$ through the capacitive and inductive parasitics, generating IMD3 products which will vary with frequency. Transistor $\mathrm{M_2}$ along with the gate voltage $\mathrm{V_{G2}}$ are designed to supply an appropriate drain voltage for $\mathrm{M_1}$ such that its g_{m2} coefficient and second-order nonlinear current are close to zero. $\mathrm{M_2}$ also lowers the impedance at the drain of M_1 thereby reducing the voltage swing at that node as well as the amount of (frequency-dependent) feedback to the gate of M_1 through its gate-drain parasitic capacitance C_{gd}. This improves the high frequency response and reduces the second-order harmonic signal that appears at the gate of $\mathrm{M_1}$ which can mix with the fundamental tone (again through $g_{m2}v_{GS}^2$) yielding IMD3. Furthermore, the $\mathrm{M_1}$-$\mathrm{M_2}$ cascode allows the use of a higher supply voltage for a larger RF output swing and power level.

The amplifier uses shunt-shunt feedback through $\mathrm{R_F}$ and $\mathrm{C_F}$ for flat wideband operation and to help with impedance matching at the input and output ports. Table I summarizes the transistor gate dimensions, capacitor values and resistor values used in the design of the PA. All of these devices are integrated on-chip, using poly resistors, and metal-insulator-metal (MIM) capacitors. Transistors $\mathrm{M_2}$ and $\mathrm{M_{2A}}$ are 3.3 V thick-oxide IO devices for reliable operation with a 2.5 V supply and large output voltage swings.

III. EXPERIMENTAL RESULTS

The proposed broadband PA was fabricated in 130 nm CMOS process and a photograph of the IC is shown in Fig 2. It occupies a total area of 0.425 mm^2 including bonding pads and decoupling capacitors, while the core circuit area is only 0.022 mm^2.

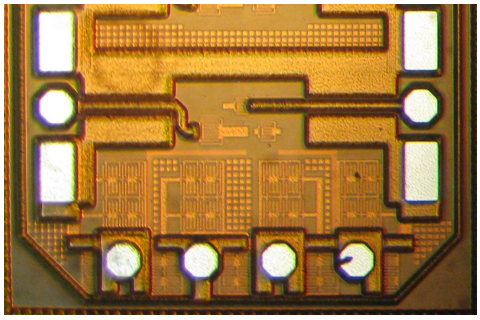

Fig. 2. Photograph of the fabricated CMOS PA.

The broadband PA was measured directly on-wafer using 40GHz coplanar waveguide (CPW) probes and DC probes. An external bias tee was used at the PA output (Fig. 1) followed by an attenuator to avoid driving the spectrum analyzer and power meter at excessively high power levels.

Fig. 3 shows the measured gain, $\mathrm{P_{SAT}}$ and $\mathrm{OP_{1dB}}$ from 1 GHz to 6 GHz. The measured gain is above 14 dB up to 4 GHz, and exceeds 12 dB at 6 GHz. $\mathrm{P_{SAT}}$ is flat over the frequency band varying by less than 1 dB between +17 dBm and +18 dBm. The measured $\mathrm{OP_{1dB}}$ is higher than +15.5 dBm over the entire bandwidth, reaching a maximum value of +16.8 dBm. The mean value is +16.3 dBm and the variation is less than $\pm$0.8 dBm from 1 GHz to 6 GHz.

Two-tone measurements were also carried out for output power levels ranging from +7 dBm to +16 dBm ($\mathrm{OP_{1dB}}$) over the 1 GHz to 6 GHz frequency band. Fig. 4 shows the output third-order intermodulation (IM3) distortion and OIP3 at 3 GHz, 4 GHz and 5 GHz versus the total output power ($\mathrm{P_{OUT}}$). At 4 GHz, the observed IM3 is better than 40 dBc at +9 dBm and higher than 30 dBc at +13.1 dBm (i.e 3.4 dB backoff from $\mathrm{OP_{1dB}}$ = +16.5 dBm). The corresponding OIP3 values are higher than +26.4 dBm at +9 dBm output power and higher than +25.1 dBm at +13.1 dBm. Similar results are seen at 3 GHz and 5 GHz. Fig. 5 shows the IM3 and OIP3 at 4 dB backoff from $\mathrm{OP_{1dB}}$ from 1 GHz to 6 GHz. In this case, the measured IM3 and

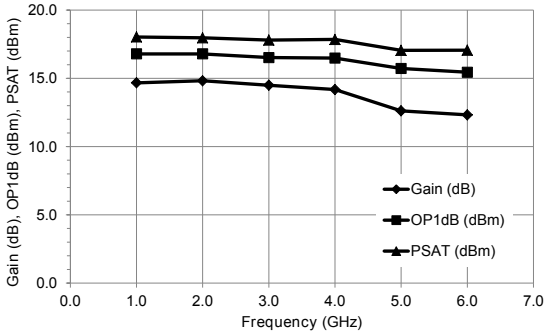

Fig. 3. Measured gain, $\mathrm{P_{SAT}}$ and $\mathrm{OP_{1dB}}$ from 1 to 6 GHz.

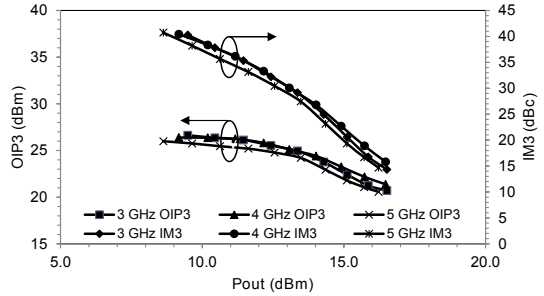

Fig. 4. Measured IM3 and OIP3 versus P_{OUT}

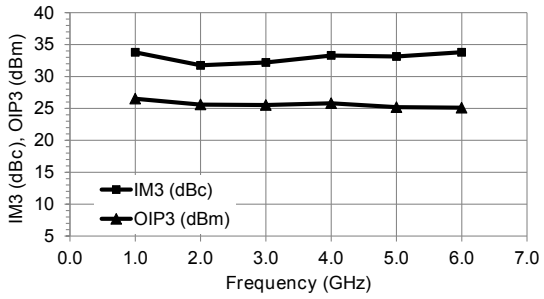

Fig. 5. Measured IM3 and OIP3 from 1 GHz to 6 GHz.

OIP3 are better than 31.8 dBc and +25.1 dBm respectively up to 6 GHz. Overall, an IM3 better than 30 dBc and an OIP3 better than +25 dBm were achieved from 1 GHz to 6 GHz at power levels reaching +12 dBm or 4 dB backoff from OP_{1dB}.

Table II summarizes the performance of this PA with that of other broadband CMOS PAs reported in the literature [12]–[14].

IV. Conclusion

Reducing the sensitivity of the DS method to RF frequency and power level is critical for widespread industrial use in broadband applications. The DS method is advantageous for linearizing monolithic amplifiers because it requires very little additional space on-chip. In this paper we demonstrated a CMOS PA that employs DS with cascode transconductors to achieve low second- and third-order distortion for high OIP3. The OIP3 performance is maintained over a broad range of frequencies and power levels without re-adjusting the bias.

TABLE II
Summary of Broadband PA Characteristics

Characteristic	**This work**	[12]	[13]	[14]
CMOS Process	**130 nm**	180 nm	90 nm	180 nm
Area (mm^2)	**0.022**	0.684	0.697	0.414
Freq. (GHz)	**1–6**	1–5	5.2–13	0.1–1.2
P_{SAT} (dBm)	**18**	20–22	25.2	19.5–20.5
Gain (dB)	**13.5±1.2**	15–20	18.5	22.5±2.5
OP_{1dB} (dBm)	**16.3**	18–20	22.6	17.1–19.1
OIP3 (dBm)	**25.6**	–	see note[1]	see note[2]
PAE (%)	**44.3**	18–36	21.6	19.5–27

[1] >25 dBc third-order harmonic distortion at OP_{1dB}.
[2] 24 dBc IM3 at an input power level of -10 dBm.

Acknowledgment

The authors would like to acknowledge the products and services provided by CMC Microsystems, including CAD tools and chip fabrication services. Ahmed EI-Gabaly was the recipient of an NSERC Doctoral Graduate Scholarship for the period 2009 to 2011.

References

[1] K. Onizuka, H. Ishihara, M. Hosoya, S. Saigusa, O. Watanabe, and S. Otaka, "A 1.9 GHz CMOS power amplifier with embedded linearizer to compensate AM-PM distortion," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1820–1827, Aug. 2012.

[2] J. Son, I. Kim, S. Kim, and B. Kim, "Sequential digital predistortion for two-stage envelope tracking power amplifier," *IEEE Microw. Compon. Lett.*, vol. 23, no. 11, pp. 620–622, Nov 2013.

[3] K.-Y. Kao, Y.-C. Hsu, K.-W. Chen, and K.-Y. Lin, "Phase-delay cold-FET pre-distortion linearizer for millimeter-wave CMOS power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4505–4519, Dec 2013.

[4] K.-J. Cho, J.-H. Kim, and S. Stapleton, "A highly efficient doherty feedforward linear power amplifier for W-CDMA base-station applications," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 1, pp. 292–300, Jan. 2005.

[5] J. Legarda, J. Presa, E. Hernandez, H. Solar, J. Mendizabal, and J. Penaranda, "An adaptive feedforward amplifier under "maximum output" control method for UMTS downlink transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 8, pp. 2481–2486, Aug. 2005.

[6] H. Choi, Y. Jeong, C. D. Kim, and J. Kenney, "Efficiency enhancement of feedforward amplifiers by employing a negative group-delay circuit," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 5, pp. 1116–1125, May 2010.

[7] V. Aparin and L. Larson, "Modified derivative superposition method for linearizing FET low-noise amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 2, pp. 571–581, Feb. 2005.

[8] B. R. Jackson and C. E. Saavedra, "A CMOS amplifier with third-order intermodulation distortion cancellation," in *IEEE Topical Meeting Silicon Monolithic Integrated Circuits RF Systems*, Jan. 2009, pp. 1–4.

[9] J. Lee, J. Lee, B. Kim, B.-E. Kim, and C. Nguyen, "A highly linear low-noise amplifier using a wideband linearization technique with tunable multiple gated transistors," in *IEEE Radio Freq. Integr. Circuits Symp.*, June 2013, pp. 181–184.

[10] A. El-Gabaly, D. Stewart, and C. Saavedra, "2-W broadband GaN power-amplifier RFIC using the f_T doubling technique and digitally assisted distortion cancellation," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 525–532, Jan 2013.

[11] Y. Song, S. Lee, E. Cho, J. Lee, and S. Nam, "A CMOS Class-E power amplifier with voltage stress relief and enhanced efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 2, pp. 310–317, Feb 2010.

[12] P.-C. Huang, Z.-M. Tsai, K.-Y. Lin, and H. Wang, "A high-efficiency, broadband CMOS power amplifier for cognitive radio applications," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 12, pp. 3556–3565, Dec 2010.

[13] H. Wang, C. Sideris, and A. Hajimiri, "A CMOS broadband power amplifier with a transformer-based high-order output matching network," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2709–2722, Dec 2010.

[14] H. Wu, L. Wang, P. Zhou, and J. Ma, "A 0.1–1.2 GHz CMOS ultra-broadband power amplifier," in *IEEE Int. Microw. Symp.*, June 2014, pp. 1–3.