Wideband Low Noise Variable Gain Amplifier

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ABSTRACT

A low noise variable gain amplifier (LNVGA) is fully designed for operation over a wideband. Since a low noise figure (NF) and a high 1 dB compression point (P1dB), i.e. large dynamic range, is difficult to achieve in CMOS technology, gain controllability is exploited to increase the overall system dynamic range. The LNVGA is composed by a low noise amplifier (LNA) stage and a voltage variable attenuator (VVA) stage. The former aims to keep the NF low, and the latter aims to provide a very large gain variation. Also, an output buffer is used to allow for measurement with 50 Ω probes. In addition, a novel Active Balun topology is proposed which achieves competitive results for magnitude imbalance and phase imbalance. The LNVGA simulation results show a gain control range of 47.7 dB, its voltage gain varies from -26.7 dB to 21 dB, the minimum NF is 3.43 dB, the IIP3 is -4.6 dBm, and a band of operation from 200 MHz to 3.5 GHz.

Categories and Subject Descriptors

B.4 [**Very Large Scale Integration Design**]: Analog and Mixed-Signal Circuits—*Radio Frequency and Wireless Circuits*

General Terms

Design

Keywords

LNA - low noise amplifier, noise cancellation, gain variation, Active Balun, moderate inversion, dynamic range

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1. INTRODUCTION

New RF applications focused on wideband and spectrum sharing are requiring RF circuits to be highly linear as well as low noise, i.e. large dynamic range. However, the trade-off noise-linearity imposes limitations on improvements for both characteristics [1].

A widely used solution to improve RF-receivers dynamic range is to employ variable gain amplifiers (VGA), but it is usually done on lower frequencies (baseband) due to CMOS parasitics capacitances that limit the operation at gigahertz frequencies. The gain variation can be achieved by: resistive lumped-elements [2] which leads to a VGA with a high NF, phase cancelation [3] which leads to a high power consumption, and changing the transistor bias voltage [4, 5] which leads to a small gain variation.

Hence, in order to decouple that trade-off a wideband circuit with variable gain and low noise figure is proposed in this paper. When the circuit receives small signals, the gain is set to a high value which minimizes the noise contribution from the circuit and allows for a high sensitivity. On the other hand, while receiving strong signals the gain is set to a negative value, to attenuate the incoming signal and to avoid signal compression.

This paper is organized as follows. Section 2 describes the main characteristics of the circuit designed. Section 3 shows the results from extracted layout simulation. Finally, Section 4 summarizes the main contribution of this paper.

2. CIRCUIT DESIGN

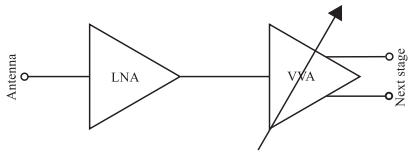
2.1 General Concept

The LNVGA circuit has two constituent blocks: a low noise amplifier (LNA) and a voltage variable attenuator (VVA) as shown in Figure 1(a). The combination of a LNA and a VVA aims to provide a low NF when the input signal is weak, which allows for a higher sensitivity; and to attenuate strong signals.

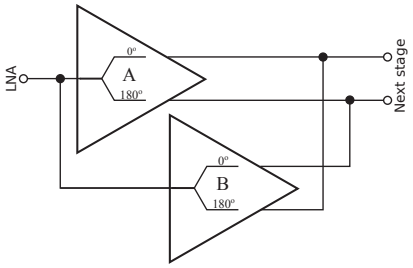
According to Friis equation [6], the main contribution to the total NF comes from the first stage, and the first stage gain mitigates the noise contribution from the following stages. Thereby, the first stage is a LNA which provides

the necessary low NF and an average gain.

The VVA, shown in Figure 1(b), consists of two Active Baluns whose differential output terminals are cross-connected to carry out a current subtraction operation. Maximum gain is obtained when balun A is turned on and balun B is turned off−an approach that helps to reduce the overall power consumption of the chip. Meanwhile, minimum gain is obtained when both baluns are fully turned on and the output currents fully cancel at the output terminal.



(a) LNVGA diagram.



(b) VVA diagram.

Figure 1: Block diagram of the LNVGA circuit (a). VVA composed by two baluns (b).

2.2 Low Noise Amplifier

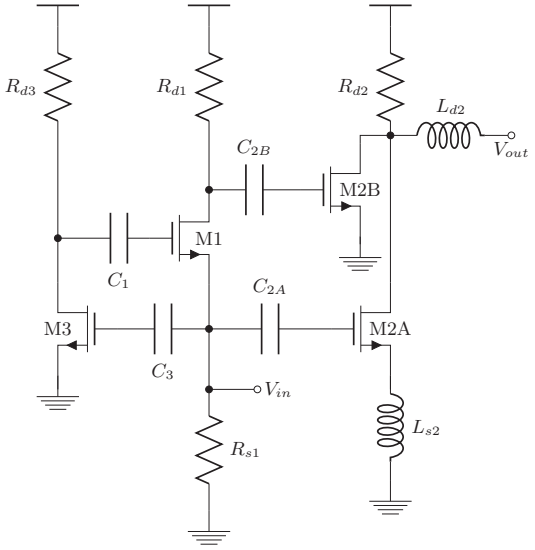
The LNA designed in this work (Figure 2(a)) combines g_m-boosting [5] and noise-cancelling [7] techniques. The former allows for a lower M1 transconductance (g_{m1}), which saves power, and the latter provides a low NF over a wide band and also decouples the trade-off between NF and input matching.

For impedance matching in this class of amplifiers the transconductance g_{m1} of M1 is usually made equal to $1/R_S$ where R_S is the signal source resistance. If R_S is 50 Ω this would require that $g_{m1} = 20$ mS, which is a large value for a single device to deliver. Using transistor M3 in a local feedback configuration helps to boost the overall transconductance seen at the source of M1 to $G_{m1} = g_{m1}\,(1 + g_{m3}R_3)$.

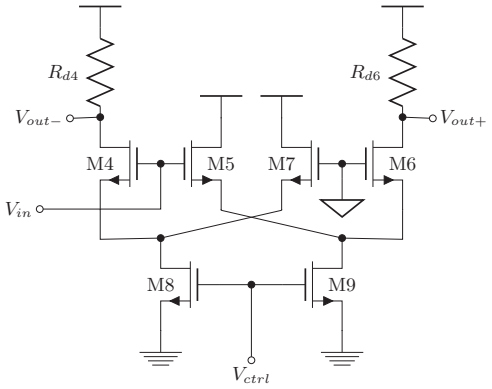
Noise-cancelling is done by a secondary amplification path that adds the signal but subtracts the noise from the matching transistor [8], thereby the amplification through both paths must be the same, which results in

$$G_{m1}R_1 g_{m2B}R_{d2} = g_{m2A}R_{d2} \Rightarrow \quad G_{m1}R_{d1} = \frac{g_{m2A}}{g_{m2B}} = \Gamma_{noise}. \quad (1)$$

Despite being very effective to cancel the noise from M1 and M3, the noise contribution from M2A and M2B are not



(a) LNA schematic.



(b) Balun schematic.

Figure 2: LNA (a) and Balun (b) schematics (BIAS not shown).

cancelled. Hence, the noise factor (F) equation is,

$$F = 1 + \left(\frac{\gamma}{\alpha}\right)\frac{1}{g_{m2A}R_S} + \left(\frac{\gamma}{\alpha}\right)\frac{g_{m2B}}{g_{m2A}^2 R_S} + \left(\frac{g_{m2B}}{g_{m2A}}\right)^2 \frac{R_{d1}}{R_S} + \frac{1}{g_{m2A}^2 R_S R_{d2}}. \quad (2)$$

The F can be converted to NF by $NF = 10\log_{10}(F)$. The noise cancelling will work for every Γ_{noise} that meets the condition from (1). However, the F will not be the same for every Γ_{noise} due to the different contribution from M2A and M2B, as presented in (2). Hence, an optimization was done sweeping Γ_{noise} for different g_{m2B}. Figure 3 presents the calculated results. The chosen operation point is $\Gamma_{noise} = 14$ and $g_{m2B} = 5$ mS because it leads to a NF around 2 dB and a smaller amplification from M2B improves its linearity, as well as the linearity from the main circuit. After optimization through simulation, $\Gamma_{noise} = 14.4$ and $g_{m2B} = 5.94$ mS.

The poles, zeros and voltage gain are calculated through the circuit transfer function. In order to improve the accu-

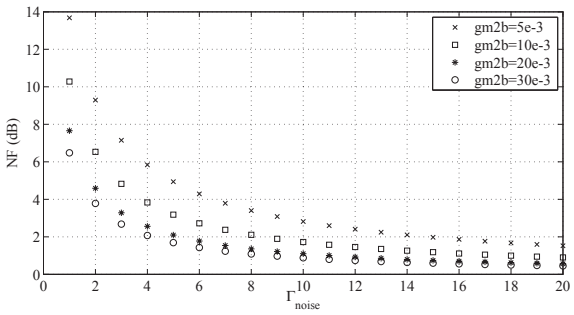


Figure 3: LNA NF calculated for different values of Γ_{noise}, at $\gamma = 4/3$ [9], $\alpha = 0.8$ [9].

racy the drain-to-source conductance from M2A (g_{ds2A}) is included in the transfer function, presented in (3). Where $R_{dout} = R_{d2} \parallel (1/g_{ds2A})$, C_{L1} is input capacitance from the second stage, i.e. the VVA, C_{gs1}, C_{gs2B}, are, respectively, the gate-to-source capacitances from M1 and M2B, and g_{m2A} is the transconductance from transistor M2A.

In order to save power, the transistors are biased in moderate inversion (MI). Besides reducing power consumption, MI-transistors can achieve a low noise figure [10], and also a good linearity [11]. However, in order to design the circuit in MI, it is necessary a methodology which covers all-inversions regions of the MOSFET. Within all-region design methodologies, the g_m/I_D [12, 13] seems to be the most suitable because all characteristics of the MOSFET can be extracted as a function of the g_m/I_D, whichever the frequency [10].

Table 1 shows the g_m/I_D chosen for each transistor, in an 130nm RF CMOS process, from which the transistors are sized.

However, under these g_m/I_D conditions the transistor size increases, thereby the parasitic capacitances which shrinks the bandwidth and reduces the input matching at frequencies higher than 1 GHz. Both problems are fixed using inductors; L_{d2} at the LNA output move for further frequencies the output pole extending the bandwidth, and L_{s2} at M2A source resonates out some parasitic capacitances, causing input matching at high frequencies to improve.

Table 1: LNA and Balun parameters.

	g_m/I_D	W (μm)	L (μm)		
M1	13.2	20	0.12	R_{d1}	600 Ω
M2A	16.9	360	0.18	R_{d2}	80 Ω
M2B	17.86	30	0.13	R_{d3}	400 Ω
M3	13.05	22	0.12	R_{s1}	1.22 kΩ
M4, M6	15.86	85	0.12	R_{d4}, R_{d6}	200 Ω
M5, M7	14.41	120	0.12	L_{d2}	6.6 nH
M8, M9	3.46	30	0.18	L_{s2}	468 pH

2.3 Voltage Variable Attenuator

As presented in section 2.1, the VVA is a single-to-differential circuit composed by two identical baluns (Figure 2(b)). Since one balun has fixed gain and another has a variable gain, the control voltage (V_{ctrl}) of the former is set to 0.8 V and the V_{ctrl} of the latter ranges from 0 V to 0.8 V; the VGA overall gain is maximum at $V_{ctrl} = 0$ and minimum at $V_{ctrl} = 0.8$.

A well known Active Balun is a differential pair where one of the inputs is AC grounded. Ideally, the RF signal goes through both differential pair branches with the same magnitude, but out-of-phase. However, the balance of the differential output is limited by the finite parasitic impedances on tail transistor and the C_{gd} on differential pair transistors.

To improve the balance, an auxiliary crossed pair is used, as shown in Figure 2(b). The proposed solution tackles the imbalance due to the finite parasitic impedances on tail transistor, thus C_{gd} is neglected. Furthermore, the transfer functions for the negative and positive outputs are (4) and (5), respectively. Where g_s and C_s are, respectively, the parasitic conductance and capacitance at the drain of M8 and M9, C_{gs4} and C_{gs5} are the gate-to-source capacitances from M4 and M5, respectively, C_{L2} is the input capacitance from the measurement buffer and $R_L = R_{d4} = R_{d6}$. In addition, transistors M4 and M6 are equal, as well as transistors M5 and M7.

Moreover, the pair M5 and M7 have a higher transconductance because their drains are not connect to a load, which turn g_s negligible and reduces the difference between (4) and (5). The imbalance due to C_s is reduced by biasing M5 and M7 in MI and M8 and M9 in SI. Since a transistor biased in MI has a larger area than one biased in strong inversion (SI), its parasitic capacitances are larger, hence $C_{gs5} >> C_s$.

The NF from the VVA was not calculated since, as told in section 2.1, the noise contribution from this block will be mitigated by the LNA. In order to get a good linearity, the transistors M4 and M6 are biased as close as possible to the bias point where the third order intermodulation product (IM3) is zero [11].

In table 1 the g_m/I_D of the balun transistors are presented. Again, the transistors are biased to operate in MI, except for M8 and M9 which are biased in SI.

3. RESULTS

The results presented in this section are all from extracted layout simulation, and measurements will be performed when the chip returns from fabrication. The circuit layout is presented in Figure 4.

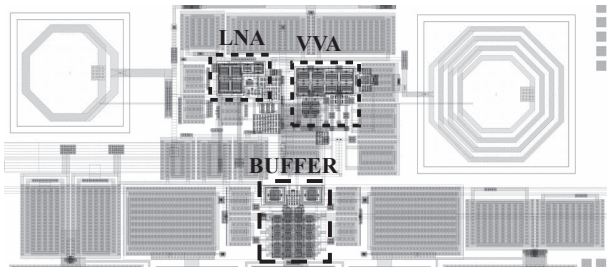


Figure 4: LNVGA core layout.

In Figure 5 the results when the circuit is at the maximum gain mode are presented. Since a measurement buffer is used in the actual circuit, the S21 results are different than voltage gain results - its difference is about 9dB. The voltage gain takes into account the amplification of the circuit without the buffer and the S21 parameter is for the circuit with the output buffer.

In addition, the circuit can keep a flat gain from 200 MHz to 3.5 GHz, which is a very wide band, its gain variation

$$H^{LNA}(s) \approx \frac{-2g_{m2A}R_{dout}}{(C_{gs1}R_{d3}s+1)(C_{gs2B}R_{d1}s+1)(C_{L1}L_{d2}s^2+C_{L1}R_{dout}s+1)}. \quad (3)$$

$$H_n^{balun}(s) \approx -\frac{g_{m4}(g_{m5}+g_s)R_L\left(\frac{C_{gs5}+C_s}{g_{m5}+g_s}s+1\right)}{(g_{m4}+g_{m5}+g_s)(sC_{L2}R_L+1)\left(\frac{C_{gs4}+C_{gs5}+C_s}{g_{m4}+g_{m5}+g_s}s+1\right)}. \quad (4)$$

$$H_p^{balun}(s) \approx \frac{g_{m4}g_{m5}R_L\left(\frac{C_{gs5}}{g_{m5}}s+1\right)}{(g_{m4}+g_{m5}+g_s)(sC_{L2}R_L+1)\left(\frac{C_{gs4}+C_{gs5}+C_s}{g_{m4}+g_{m5}+g_s}s+1\right)}. \quad (5)$$

is below 1 dB. Over that wideband, the circuit manage to keep a NF below 4.85 dB, and below 4 dB from 300 MHz to 3 GHz. The minimum achieved NF is 3.43 dB, around 700 MHz. The S11 is below -10 dB from 300 MHz to 3.38 GHz, if the flat gain band is considered, the S11 is below -8 dB which still acceptable as a matched input.

The main feature of this circuit is the large gain variation while keeping the gain flat over a wide band. This feature is presented in Figure 6.

Figure 6(a) shows the gain variation, the NF and S11 as a function of the control voltage for the LNVGA. The voltage gain ranges from -26.72 dB to 20 dB; S11 remains almost fixed and below -10 dB; the NF rises as the attenuation increases, since the NF contribution from the the buffer is larger when the gain is smaller. Hence, when using the LNVGA on a receiver chain, the next block is not allowed for a high NF. In addition, the NF being high on the maximum attenuation mode may not be a problem because this mode is only used for very strong signal and far above the noise floor. Figure 6(b) shows the gain flatness achieved by the circuit, the worst flatness happens on maximum attenuation mode and it is about 2 dB variation over entire band.

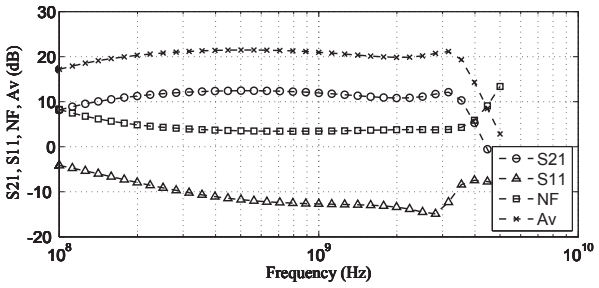
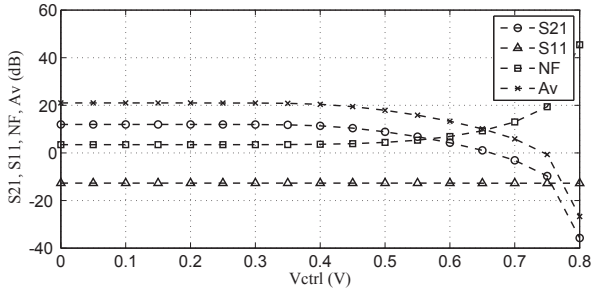


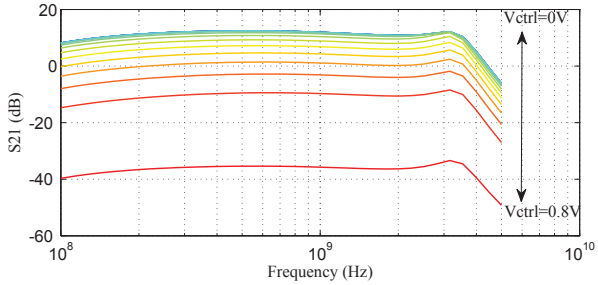
Figure 5: S21, S11, NF and voltage gain when circuit is on maximum gain mode.

The large gain variation achieved by the LNVGA can be explained by the low imbalance achieved by the proposed Active Balun, which is presented in Figure 7. These results are competitive with prior works, like [14–18], presented in table 7.

The IIP3 and P1dB results are presented on figure Figure 8. IIP3 variation over V_{ctrl} happens because the transistors from Balun B changes its operation region as V_{ctrl} sweeps. Hence, the nonlinearities from Balun A and Balun B may add themselves constructively, when V_{ctrl} =0.45 V, or destructively, when V_{ctrl} =0.8 V. P1dB also changes over V_{ctrl}.



(a)



(b)

Figure 6: Parameters variation with the V_{ctrl} for 1 GHz (a) and S21 variation with V_{ctrl} over the entire band (b).

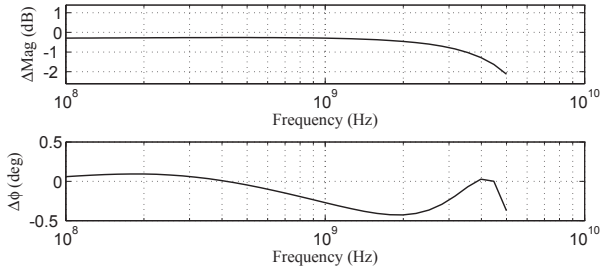


Figure 7: Magnitude (ΔMag) and Phase ($\Delta\phi$) imbalance.

The best IIP3 is -4.6 dBm, when V_{ctrl} = 0.45 V, and the best P1dB is -13.52 dBm, when V_{ctrl} =0.7 V.

Table 3 shows a comparison with prior amplifiers with

Table 2: Balun results in comparison to other works.

REF.	[15]*	[14]*	[16]†	[17]*	[18]*	This work †
Mag. imb. (dB)	1.5	±0.3	0.2	0.5	1.3	1.28
Phase imb. (deg)	8	±2	6	5	1.6	0.4
BW (GHz)	0.5-8	0.3-3.5	0.1-5	0.1-2	4.6-5.7	0.1-4

†Simulated results.
* Measured results.

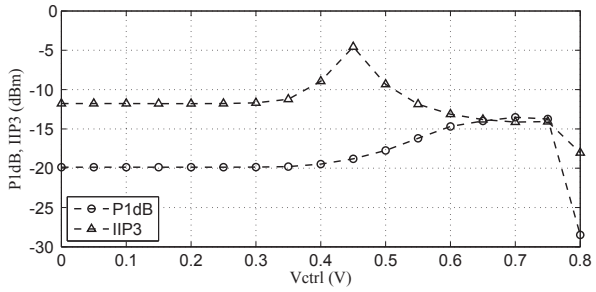


Figure 8: P1dB and IIP3 results for 1 GHz.

the variable gain feature. The gain variation achieved by our LNVGA is the second largest one, about 47.7 dB. The IIP3 achieved by our LNVGA is below -4.6 dBm because it is composed by two stages and the IIP3 from the second stage, i.e. the VVA, is not high enough to compensate the gain from the LNA.

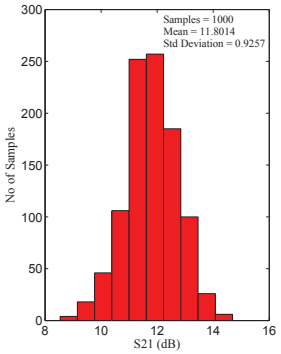
The overall power consumption is 19 mW at V_{ctrl} =0 V and 29 mW at V_{ctrl} =0.8 V. The techniques introduced on the LNA to save power worked well, the LNA consumes only 7.9 mW, which is considerable low for a wideband circuit. However, the crossed-pair technique introduced on the Active Balun to improve their output balance increases the VVA power consumption. The VVA consumes 10.4 mW at V_{ctrl} =0 V and 20.8 mW at V_{ctrl} =0.8 V. The bias circuits consumes about 0.5 mW.

Table 3: LNVGA results in comparison with prior works.

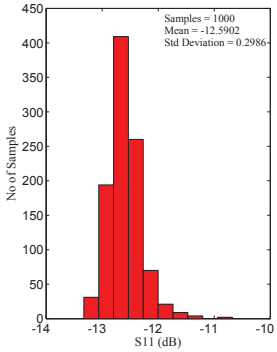
REF.	[4]*	[3]*	[2]*	[5]*	This Work†
Gain (dB)	[-10, 8]	[-30, -2.6]	[-10, 50]	[-5, 11]	[-26.7, 21]
Flatness (dB)	2	3	2.5	3	2
Min. NF (dB)	4.2	-	17	3.2	3.43
IIP3 (dBm)	1.8	3	-3.4 - -45.4	0	-4.6
BW (GHz)	[0.03, 7]	[1, 3.5]	[0.01, 2.2]	[1, 5]	[0.2, 3.5]
Power (mW)	9	18	2.5	19	19
Area (mm^2)	1.16	0.05	0.01	0.067	0.173

†Simulated results.
* Measured results.

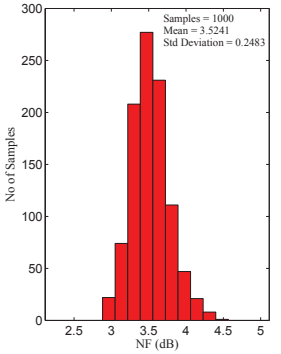
Figure 9 presents the results from Monte Carlo simulation for process variation. The variation of NF and S11 are below 0.3 dB, so that the noise canceling structure still work well despite the process variation. The S21 variation is about 0.92 dB, which means the circuit gain remains flat in spite of the process variation. The Monte Carlo results for IIP3 has a spread from -14 dBm to -8 dBm and its deviation is about 1.6 dBm. These results are explained due to the transistors from the LNVGA are biased at MI region, inside this region the third derivate from the drain current, i.e. third order coefficient, has a very sharp variation. Hence, process variation damages our circuit IIP3.



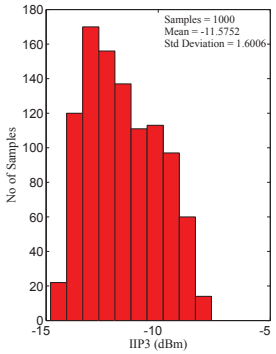
(a) Monte Carlo results for S21.



(b) Monte Carlo results for S11.



(c) Monte Carlo results for NF.



(d) Monte Carlo results for IIP3.

Figure 9: Monte Carlo results for process variation when $V_{ctrl} = 0$ V and at 1 GHz.

4. CONCLUSION

A LNVGA has been developed in IBM 130nm RF CMOS process. The occupied area is about 0.173 mm^2 and the consumed power is 19 mW from 1.2V power supply at the maximum gain control. The LNVGA has achieved a very large and flat gain variation, 47.7 dB. The NF remains below 4 dB from 300 MHz to 3 GHz and its minimum value is 3.43 dB. Also, a good input match over the entire band is achieved and the maximum IIP3 achieved is -4.6 dBm.

5. ACKNOWLEDGMENTS

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6. REFERENCES

[1] F.D. Baumgratz, S.B. Ferreira, and S. Bampi. RF system level design for a Spectrum Sensing Receiver. In *Electronics, Circuits, and Systems (ICECS), 2013 IEEE 20th International Conference on*, pages 771–774, Dec 2013.

[2] Yanjie Wang, B. Afshar, Tuan-Yi Cheng, V. Gaudet, and A.M. Niknejad. A 2.5mW inductorless wideband

VGA with dual feedback DC-offset correction in 90nm CMOS technology. In *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE*, pages 91–94, June 2008.

[3] C.E. Saavedra and B.R. Jackson. Voltage-variable attenuator MMIC using phase cancellation. *Circuits, Devices and Systems, IEE Proceedings* , 153(5):442–446, October 2006.

[4] F. Zhang and P. Kinget. Low power programmable-gain CMOS distributed LNA for ultra-wideband applications. In *VLSI Circuits, 2005. Digest of Technical Papers. 2005 Symposium on*, pages 78–81, June 2005.

[5] A. M. El-Gabaly and C. E. Saavedra. Wideband variable gain amplifier with noise cancellation. *Electronics Letters*, 47(2):116–118, 2011.

[6] Behzad Razavi. *RF Microelectronics*. Pearson, second edition, 2012.

[7] Chih-Fan Liao and Shen-Iuan Liu. A broadband noise-canceling CMOS LNA for 3.1-10.6-GHz UWB receiver. In *Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005*, pages 161–164, Sept 2005.

[8] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta. Wide-band CMOS low-noise amplifier exploiting thermal noise canceling. *Solid-State Circuits, IEEE Journal of*, 39(2):275–282, 2004.

[9] Jusung Kim, S. Hoyos, and J. Silva-Martinez. Wideband common-gate cmos lna employing dual negative feedback with simultaneous noise, gain, and bandwidth optimization. *Microwave Theory and Techniques, IEEE Transactions on*, 58(9):2340–2351, 2010.

[10] R. Fiorelli, F. Silveira, and E. Peralias. MOST Moderate-Weak-Inversion Region as the Optimum Design Zone for CMOS 2.4-GHz CS-LNAs. *Microwave Theory and Techniques, IEEE Transactions on*, 62(3):556–566, March 2014.

[11] B. Toole, C. Plett, and M. Cloutier. RF circuit implications of moderate inversion enhanced linear region in MOSFETs. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 51(2):319–328, Feb 2004.

[12] F. Silveira, D. Flandre, and P.G.A. Jespers. A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA. *Solid-State Circuits, IEEE Journal of*, 31(9):1314–1319, Sep 1996.

[13] Alessandro Girardi and Sergio Bampi. Power constrained design optimization of analog circuits based on physical gm/id characteristics. In *Proceedings of the 19th Annual Symposium on Integrated Circuits and Systems Design*, SBCCI '06, pages 89–93, New York, NY, USA, 2006. ACM.

[14] S.C. Blaakmeer, E.A.M. Klumperink, B. Nauta, and D.M.W. Leenaerts. An inductorless wideband balun-lna in 65nm cmos with balanced output. In *Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European*, pages 364–367, Sept 2007.

[15] G.S.K. Yong and C.E. Saavedra. A compact capacitor compensated wideband balun in cmos technology. In *Communications, 2008 24th Biennial Symposium on*, pages 306–309, June 2008.

[16] Lu Zhang, Chao Chen, and Jianhui Wu. A 100-mhz - 5.0-ghz active balun using 0.18-um cmos process. In *Electron Devices and Solid-State Circuits (EDSSC), 2011 International Conference of*, pages 1–2, Nov 2011.

[17] Jusung Kim and J. Silva-Martinez. Wideband Inductorless Balun-LNA Employing Feedback for Low-Power Low-Voltage Applications. *Microwave Theory and Techniques, IEEE Transactions on*, 60(9):2833–2842, Sept 2012.

[18] Sen Wang and Chih-Hsuan Lee. Low-phase error and high isolation cmos active balun. In *Microwave Symposium (IMS), 2014 IEEE MTT-S International*, pages 1–4, June 2014.