68-73 GHz Common-Base HBT Amplifier in 55 nm SiGe Technology

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***Abstract*— The design of a common-base (CB), power-combined, SiGe BiCMOS amplifier is reported. Wilkinson couplers are used for power splitting and combining at the input and output of the amplifier. The HBTs have three emitter fingers and each finger has a length of 2.7 μm and a width of 0.18 μm. The gain of the amplifier can be externally varied by biasing the HBTs from a 1.3-1.5 V dc supply applied to their collectors through on-chip bias tees and applying 850-900mV to the bases. Measurements on the fabricated amplifier reveal that the maximum gain can be varied between 10.91 and 15.75 dB, it has a 3-dB bandwidth from 68 to 73 GHz and an OP_{1dB} of -1.8 dBm at 71 GHz. The chip area is 0.8 mm^2 and it draws a dc power between 5.2 and 18.7 mW.**

***Index Terms*— BiCMOS integrated circuits, E-band, Millimeter wave integrated circuits, amplifiers.**

I. INTRODUCTION

Technology development for E-band wireless communications links is proceeding at a fast pace. In the area of integrated circuits, a full range of components including low-noise amplifiers [1], power amplifiers [2] and mixers [3] have been reported for the 71-86 GHz band and beyond. In addition, E-band chipsets that deliver higher functionality such as I/Q modulation [4] and full receivers [5] have also been demonstrated.

This paper describes the design of a 68−73 GHz variable-gain amplifier targeted as a general-purpose gain block for an E-band frequency converter, which can be used to amplify the LO signal. The amplifier consists of two power-combined CB amplifiers in a 50-Ω environment and is designed using ST Microelectronics' 55nm SiGe BiCMOS technology. The amplifier's passive components are implemented with shielded coplanar waveguide (CPW) transmission lines.

II. CIRCUIT DESIGN

The block diagram of the complete amplifier system is shown in Fig.1. The 3-dB power coupler on the left splits the incident signal into two equal-amplitude and in-phase components that are fed to the amplifier pair. The amplifiers are identical and their design is based on a SiGe HBT with CB configuration. The second in-phase power 3-dB power coupler at the right of the diagram combines the amplified signals at the output of the circuit.

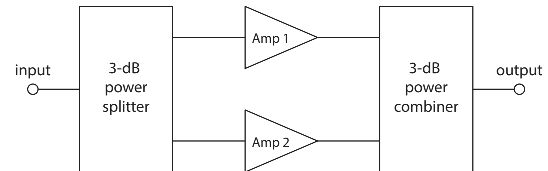

Fig. 1. Block diagram of the fully-integrated BiCMOS amplifier described in this work.

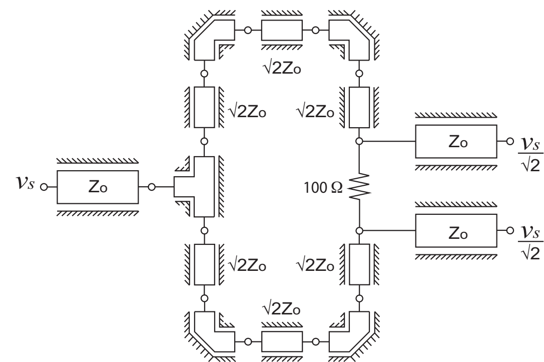

Fig. 2. Schematic of the Wilkinson couplers used in Fig. 1 for power splitting and combining (transmission line lengths not drawn to scale).

Wilkinson power couplers are used to implement the input power splitter and the output power combiner in Fig. 1 and their schematic diagram is depicted in Fig.2. The input 50-Ω transmission line has a signal-line width of 7.47 μm and a gap of 16.425 μm between the signal and ground conductors. Meanwhile, the 70.7 Ω transmission lines have a signal-line width of 2.61μm and a gap of 9.9μm.

The circuit diagram of the CB amplifier block is shown in Fig. 3 together with the component values and the device dimensions. The CB amplifier uses a single transistor, Q_1, with three emitter fingers, each with a length of 2.7 μm

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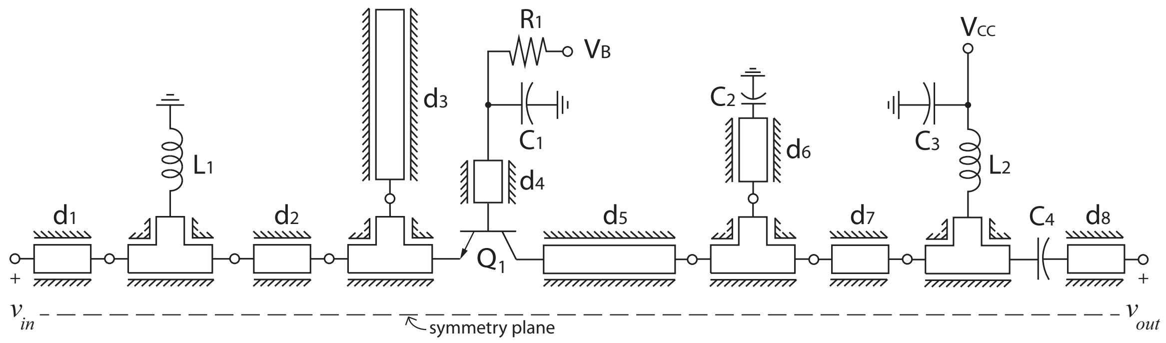

T-line	d_1	d_2	d_3	d_4	d_5	d_6	d_7	d_8	widths	gaps
length	18 μm	9 μm	277 μm	18 μm	223 μm	76.5 μm	9 μm	18 μm	7.47 μm	16.425 μm

part	L_1	L_2	R_1	C_1	C_2	C_3	C_4	HBT parameters		
value	416 pH	416 pH	5 kΩ	0.52 pF	0.34 pF	0.52 pF	0.52 pF	n_e=3	L_e=2.7 μm	W_e=0.18 μm

Fig. 3. Schematic diagram of the common-base HBT amplifiers. The amplifier in the lower-half is identical to the amplifier at the top.

and a width of 0.18 μm. The CB topology is used in this design because, for the same device size and geometry, the gain-bandwidth product of the CB configuration is significantly better than that of the common-emitter (CE) and common-collector (CC) topologies [6]. Furthermore, the real component of the input impedance at the emitter terminal in the CB topology is approximately $1/g_m$ and is thus convenient for matching the amplifier to the 50 Ω characteristic impedance used in the system.

Component L_1 in Fig. 3 is a choke inductor with a value of 416 pH that provides a path to ground for transistor's dc emitter current. Transmission line d_3 is an open-circuit matching stub with a length of 277 μm, which is approximately a quarter wavelength of the amplifier's centre frequency. Thus, the fringing capacitance at the end of the stub is transformed into an inductive reactance that is in parallel with parasitic base-emitter capacitance, C_{be}, and resonates it out.

The dc bias voltage, V_b, at the base of Q_1 is supplied through a 5 kΩ resistor. A 0.51 pF capacitor connected between the base terminal and ground is used to establish an ac ground at that node. Transmission lines d_5 and d_6 constitute the output matching network of the amplifier. The dc bias voltage, V_{CC}, at the collector terminal of the transistor is fed through an on-chip bias-tee consisting of inductor L_2 and capacitor C_3. Capacitor C_4 is an output decoupling capacitor. Both the base and collector bias voltages can be externally varied to adjust the gain of the amplifier as well as to compensate for temperature variations and simulation inaccuracies.

As noted earlier, the transmission lines are shielded CPW lines to reduce substrate losses. The capacitors are multi-finger interdigitated MOM structures implemented using top-level thick metals to reduce losses. The capacitors have a quality factor of ∼20 in the frequency band of interest.

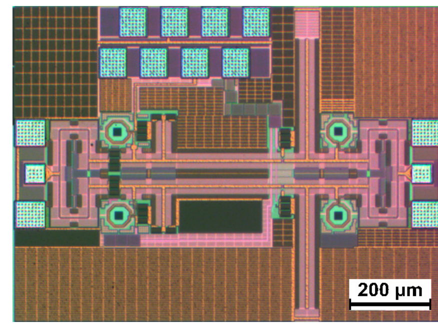

Fig. 4. Microphotograph of the fabricated 55 nm SiGe HBT amplifier.

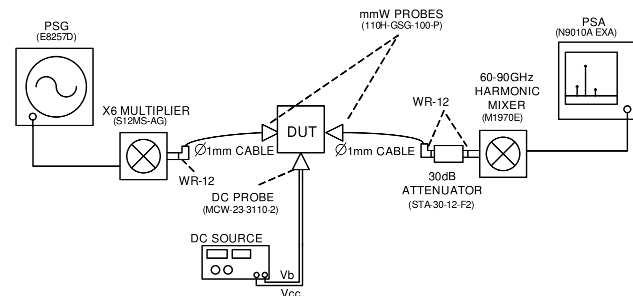

Fig. 5. Test setup used to measure the amplifier.

III. Measurements

The amplifier was fabricated using ST Microelectronics' 55 nm SiGe process and a microphotograph of the chip is depicted in Fig. 4. The die occupies an area of 0.8 mm^2 including bond pads. Shown in Fig. 5 is a block diagram

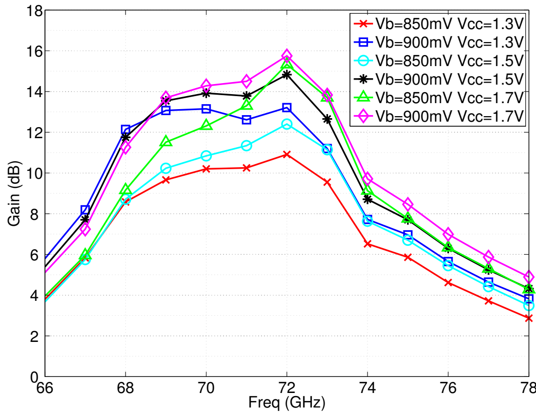

Fig. 6. Measured small-signal gain of the amplifier for different transistor base and collector bias voltages.

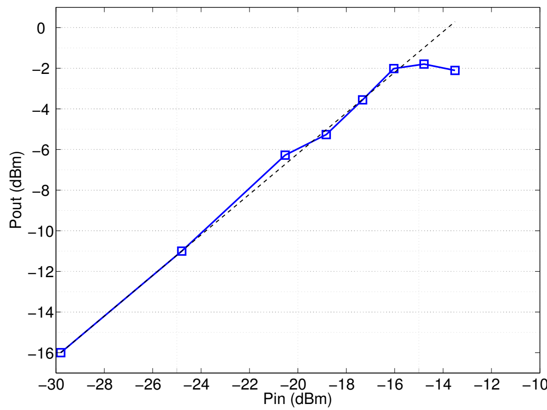

Fig. 7. Measured input-output power performance of the amplifier at 71 GHz.

of the test setup used to measure the gain and linearity response of the amplifier.

Fig. 6 shows the measured small-signal gain of the amplifier for different values of the base and collector bias voltages. The 3-dB bandwidth of the circuit ranges from 68 to 73 dB irrespective of the changes in the dc bias conditions. The peak gain of the amplifier occurs at 72 GHz and varies from 10.9 to 15.8 dB as a function of the collector voltage, yielding a gain-control range of approximately 5 dB. Table I summarizes the gain, bandwidth and DC power consumption of the chip.

The RF power response curve of the amplifier, P_{out} vs. P_{in}, measured at 71GHz is shown in Fig. 7 for the bias conditions $V_{CC} = 1.5V$ and $V_B = 900mV$. As shown, the IP_{1dB} is -14.6dBm and the OP_{1dB} -1.8dBm. At present, only simulated intermodulation distortion results are available for the amplifier. Two-tone simulations at midband reveal an IIP3 of approximately +3 dBm and an OIP3 of +12 dBm.

TABLE I
AMPLIFIER PERFORMANCE SUMMARY

V_{CC}(V)	V_B(mV)	P_{DC}(mW)	Gain(dB)	3-dB BW (GHz)
1.3	850	5.2	10.91	67.7-73.5
1.3	900	13	13.21	67.5-73.3
1.5	850	7.5	12.4	68.5-73.5
1.5	900	15	14.83	68-73.2
1.7	850	10.2	15.33	70-73.3
1.7	900	18.7	15.75	68.6-73

IV. CONCLUSION

A millimeter-wave CB amplifier stage has been presented. Measurement results show that the maximum gain can be varied between 10.91 and 15.75dB with a 3-dB bandwidth of 68-73.2GHz. The circuit is suitable as a general-purpose gain stage for the lower part of the E-band spectrum or as an LO boosting amplifier.

ACKNOWLEDGMENTS

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