A Very High-Sensitivity CMOS Power Detector for High Data Rate Biotelemetry Applications

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***Abstract*—This paper presents a microwave power detector for an on-off keying (OOK) receiver for biotelemetry. The detector is designed using 130 nm CMOS technology and it consists of a high-gain inverting amplifier biased at the edge of turn-on and a low-frequency comparator circuit. The detector is designed to operate at 7.6 GHz and simulation results show that it has a sensitivity of -55 dBm while drawing just 9.3 µA from a 1 V supply. Furthermore, the detector can operate at bit rates of up to 100Mbps.**

I. INTRODUCTION

In the design of microelectronic circuits for body area networks and related biotelemetry applications, minimizing the consumption of dc power is a dominant design constraint. One way to reduce the power draw of a biotelemetry receiver is to use a wake-up circuit (WuC) that is constantly listening for data transmissions and when a transmission is detected the WuC turns on the full receiver. A key component of the WuC is the power detector. This power detector must be able to pick up very weak microwave signals and it must also consume very low amounts of dc power. This paper is about the design and implementation of such a power detector.

In general, power detection involves taking a high frequency signal and producing a low frequency signal proportional to the amplitude or power of the input signal, from this low frequency signal the power of the RF signal is easily determined. The most basic power detection (or envelope detection) is implemented by feeding the RF signal through a rectifying diode (or transistor) and placing an RC load after the diode. The RC time constant must be short enough to tracks the changes in the RF signal's envelope yet long enough to filter out the fast RF oscillation.

For detecting very weak signals, power detectors include a frequency conversion step where the RF signal is mixed with a local oscillator (LO) tone to produce a low-frequency IF signal that is subsequently amplified. The IF goes through the standard power detector described above and knowing the conversion loss of the mixer and the gain of the amplifier, the power of the original RF signal is determined. The drawback of this approach is that the LO and mixer consume a good amount of dc power, which is inconvenient for biotelemetry systems with WuC [1].

A CMOS power detector design that has become common in recent years is shown in Fig. 1. It uses a differential amplifier topology but the RF input is connected in single-ended fashion to one of the amplifier inputs. This implementation yields a DC term proportional to the square of the input signal, while the capacitors filter out high frequency content. Analysis of the circuit is shown in more detail in [2].

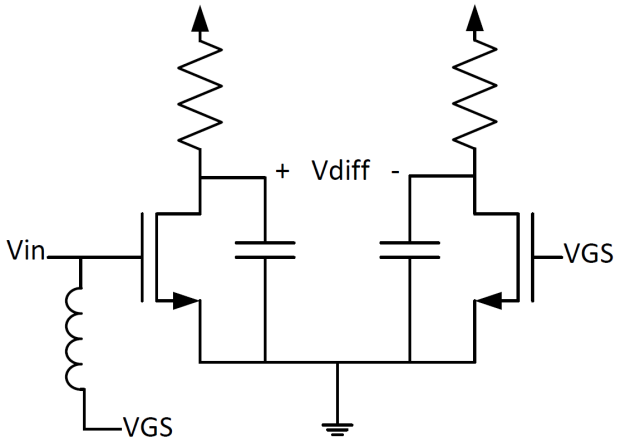

Fig 1. Typical envelope detector for low power signals.

The topology presented in this paper connects the negative output to VGS, creating a single ended output relative to the DC bias point and allowing the circuit to bias itself. What makes this circuit original is the sheer simplicity of it and the possible bit rate that comes from such simplicity.

II. CIRCUIT ARCHITECTURE

The circuit proposed in this paper is shown in Figure 2. It consists of an impedance matching network, an RF amplifier biased in the nonlinear region of its transfer function and a voltage comparator. The impedance matching circuit is a simple L-C circuit designed to resonate and maximize the RF voltage component of Vg at the input of the amplifier. The RF amplifier is intentionally biased to introduce nonlinear distortion and produce a shift in the average value of its output voltage (Va), which is detected and amplified by the voltage comparator.

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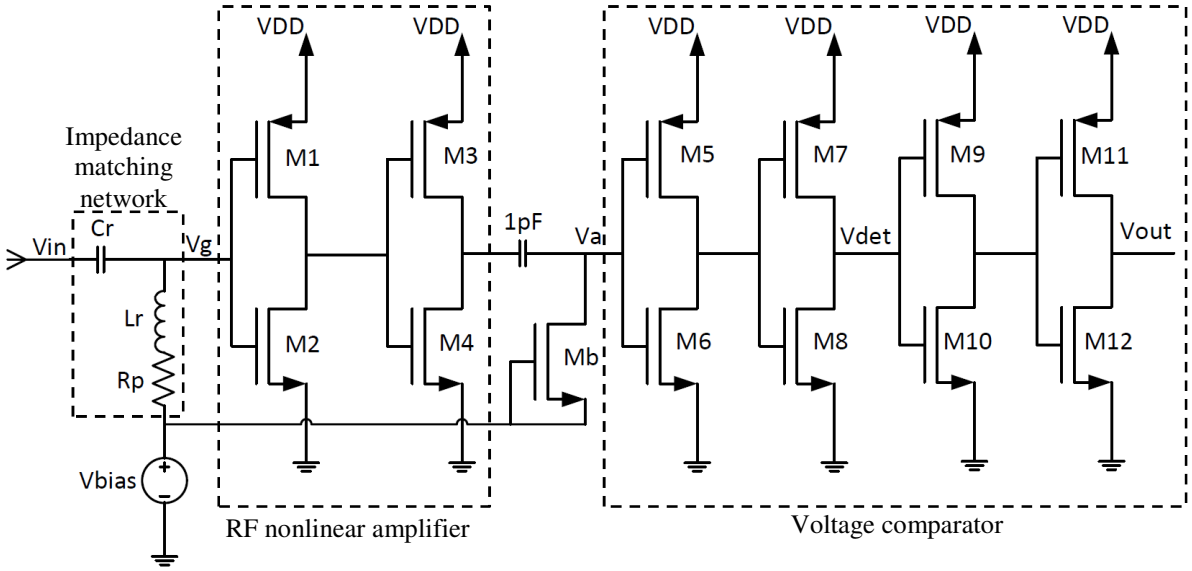

Fig 2. Overall Circuit architecture.

Using the assumption that the gate impedances of M1 and M2 in Fig. 2 are very large, the voltage expression for Vg as a function of the input RF voltage is

$$Vg = \frac{jwLr + R_P}{jwLr + R_P + \frac{1}{jwCr}} Vin \qquad (1)$$

where Rp is the parasitic resistance of inductor Lr. At resonance this reduces to Vg = (jQ_{L0} + 1)Vin, where Q_{L0} is the quality factor of inductor Lr at the resonant frequency. At 7.6 GHz, the input impedance only is given by R_P, so a large inductor is chosen to provide a 50 Ohms resistance. The passive gain for the network is found to be 6.8 V/V or 16.5 dB.

The RF nonlinear amplifier is a simple pair of cascaded CMOS inverters biased at the lower turn on point. Figure 3 shows how applying an RF signal to the input causes a shift in the average of the output voltage. This allows a high frequency signal to produce a low frequency component corresponding to its envelope, which can then be detected by the comparator stage. Both stages (M1-2 and M3-4) draw 2.1 µA of current for a total of 4.2 µA.

At 7.6 GHz, the output of M1/M2 is also affected by rise and fall times. M1 and M2 are mismatched to take advantage of this; the input to M3 and M4 falls faster than it rises and increases the shift in DC voltage level.

The transistor Mb in Figure 2 acts both as a collecting capacitor and as a high RF impedance. The nonlinear amplifier's transistors are biased for a total trans-conductance (gm) value of 40 µS, meaning the only way to achieve gain is through high total output impedance (>25 KΩ). Practically, impedance above 100 KΩ is desired here and transistor Mb provides high RF impedance while being invisible to the DC bias voltage.

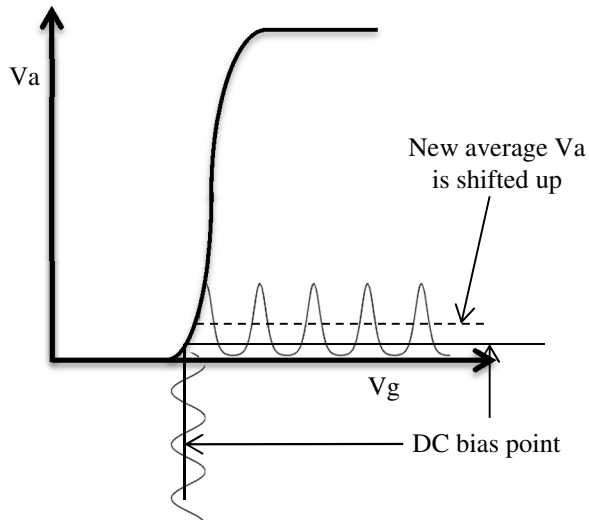

Fig 3. RF amplifier biased in its nonlinear region for envelope detection.

The voltage comparator compares the average value of Va against the threshold switching voltage of the inverter stages. This threshold voltage is indicated by the DC bias point in Fig 3. If all transistors were identical, then all inverter stages would have the same lower threshold. The Width of M5 is increased to 175 nm to shift the threshold of the DC comparator upwards. This way, the output Vout will stay tied to 0 when there is no input but will switch to logic 1 when enough power is detected. Reducing this extra threshold improves sensitivity, but also increases the risk of false detection and represents an engineering tradeoff. The transistors M5 and M6 draw 2.3 µA of DC current while M7 and M8 draw 1.8 µA. The four remaining transistors M8-M12 draw only a few nanoamps of continuous current; these inverters can be treated as a purely digital circuit.

The bias voltage Vbias is realized using 4 cascoded transistors and a 2 pF capacitor. This setup consumes 1 µW of power and is included in the 9.3 µW power total. A

resistive divider could be effective, but the bias voltage requires too low of a tolerance and determines the sensitivity of the receiver.

It would seem intuitive that the 1 pF DC blocking capacitor would also block the average shift in Va. This is not an issue in practice however; the product of the 1pF capacitance and the impedance through transistor Mb is very large compared to the intended bit period. Impedance across Mb in gigaohms yields a time constant in milliseconds, several orders of magnitude above the ten nanosecond bit period. The capacitor also has a chance to discharge whenever logic 0 is being received.

The total DC current draw is the sum of 4.2 µA for the RF amplifier, 4.1 µA for the DC comparator, and 1.0 µA for the DC biasing circuit. Using a supply voltage of 1.0 V gives a static power consumption of 9.3 µW.

III. Simulation Results

The simulated reflection coefficient, S11, is less than -40 dB at 7.6 GHz and is plotted in Fig 4. A source impedance of 50 Ohms was used for the S-parameter simulation. The inductor occupies an area of 170 x 170 um with 7.5 turns yielding a nominal value of 4.2 nH. The Capacitor is a basic 70 fF mimcap. The input network also provides 16.5 dB of passive voltage gain due to the resonant behavior of Lr and Cr.

The nonlinearity in the RF amplifier introduces an average shift in Va that increases with the amplitude of the input signal Vin. The average voltage is then fed to voltage comparator that responds to the change and amplifies it by around 100 dB, producing a signal at the digital level. The amplitude of the input voltage Vin, the resulting shift in Va, and the detection voltage Vdet are all plotted against input power in Figure 5. Figure 6 shows how the Vdet-Pin curves shift as the input frequency deviates from 7.6 GHz. The same trends are shown in Figure 7, where the detection voltage is plotted over a frequency sweep. The curves show that the circuit is tolerant to deviations in frequency. More filtering at the input could be used to sharpen the roll-off of the curves in Figure 7. The figures show that the circuit could be used for detection down to -60 dBm, but designing for that ability requires tolerance values around 0.1% in the DC bias and inverter lower threshold voltage. The detector is more practically useful down to -55 dBm.

The waveforms for Va and Vin are shown in Figure 8. The waveforms are shown for and input power of -55 dBm and a '1011' bit sequence at 100 Mbps . The average shift in Va is amplified to Vdet which drives the digital Vout, shown in Figure 9. Vin has an amplitude of 0.56 mV while Va shifts by 3.8 mV. Figure 9 shows how the detection voltage and output voltage respond to a bit sequence.

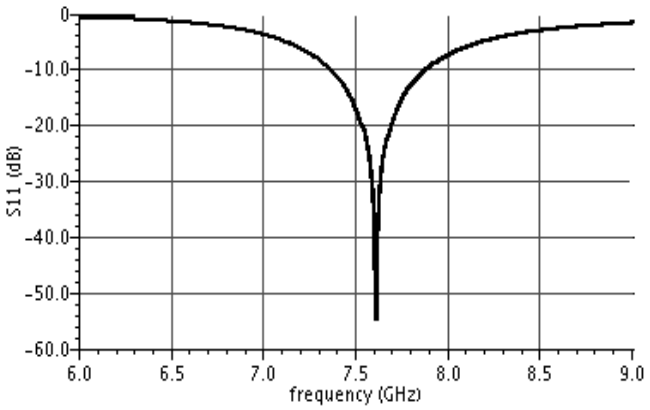

Fig 4. Reflection coefficient at input of power detector.

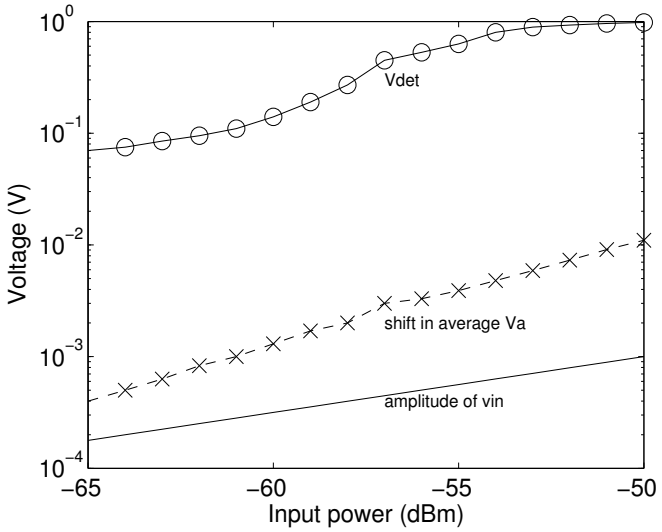

Fig 5: Vin, shift in Va, and detection voltage all plotted against input power.

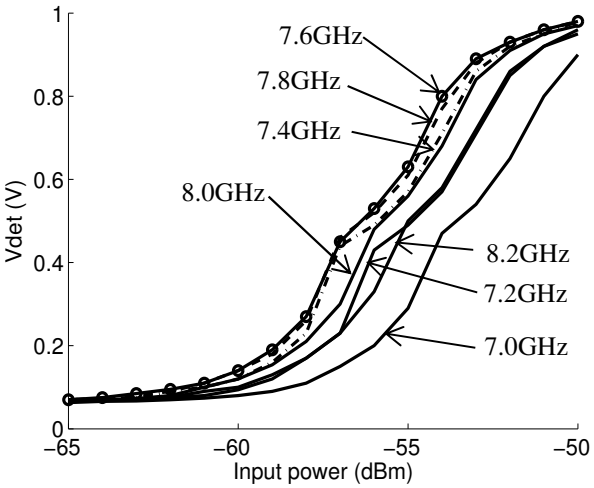

Fig 6: Dependence of detection voltage on power of input signal for different input frequencies.

Table 1 summarizes the performance of this work and compares it to other work in this field. By using envelope detection without down conversion, the maximum bit rate can be pushed extremely high. This is advantageous to reduce wake-up latency and to reduce the time required for sending the more powerful wake-up signal. This work also boasts simplicity, as no external circuitry is required and it is fabricated in a standard CMOS technology.

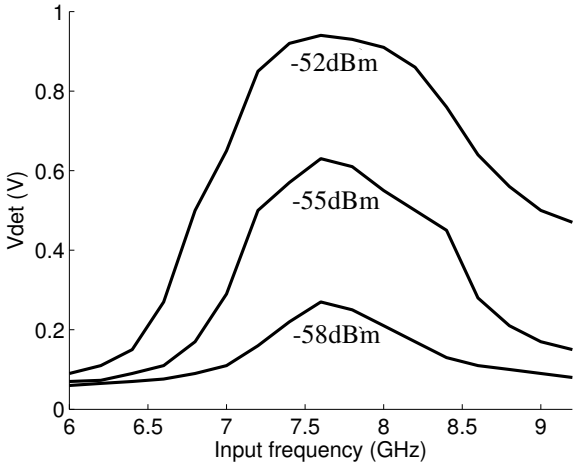

Figure 7: Dependence of detection voltage on frequency of input signal for different input powers.

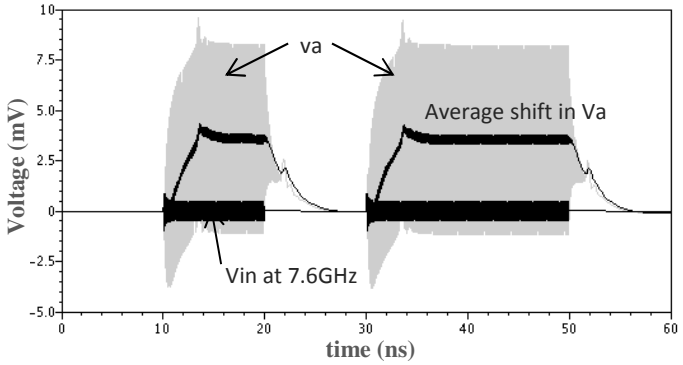

Fig 8. Waveforms for Va in response to -55dBm input power.

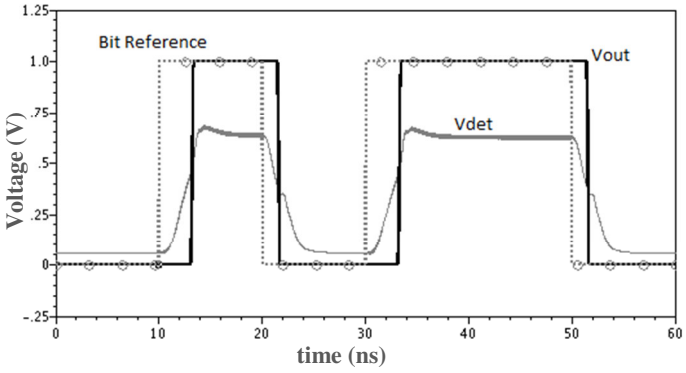

Fig 9: Digital level waveforms in response to -55dBm input power.

TABLE I. PERFORMANCE COMPARISON OF POWER DETECTORS IN WAKE-UP RECEIVERS.

Ref	*Power (µW)*	*Sensitivity (dBm)*	*Carrier Frequency (GHz)*	*Bit Rate (kbps)*	*Process (nm)*	*Chip area (mm^2)*
this work	9.3	-55	7.6	100 000	130	0.1
[1]	52	-72/-70	2.0	100/200	90	0.1*
[3]	9.0	-68	60	350	180	1.1
[4]	2.4	-71	0.868	100	130	1.15
[5]	2.3	-47	2.45	200	130	0.007**
[6]	51	-80/-75 -69/-64	0.915 2.4	10/100 10/100	90	0.36
[7]	415	-87/-82	2.4	250/500	65	0.2
[8]	20	-50	2.4	50	130	/

*Excludes off-chip bulk acoustic wave (BAW) resonator.
**Excludes several mm^2 required for RF voltage transformer and external biasing circuit.

IV. CONCLUSION

A 9.3µW wake up receiver is simulated in 130nm CMOS technology for low power wireless communications. The receiver can operate up to 100Mbps using a carrier frequency of 7.6GHz. This represents orders of magnitude improvement in possible bit rates while drawing very low power and maintaining high sensitivity.

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