+14 dB Improvement in the IIP_3 of a CMOS Active Mixer Through Distortion Cancellation

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***Abstract*— The derivative superposition (DS) technique is used to cancel the third-order intermodulation distortion (IMD) produced in a downconverter mixer. By providing separate bias currents to the mixer core and the distortion-cancelling circuitry, the IMD is reduced but the conversion gain remains nearly the same in the distortion-cancelling mixer compared to the baseline mixer without linearization. Measurements show that the distortion-cancelling mixer has an IIP_3 that is 14 dB above the IIP_3 of the baseline mixer while the conversion gain drops by only -0.7 dB. The distortion-cancelling mixer only needs an additional 2.4 mW of dc power relative to the baseline mixer's power draw. The test chip was fabricated in a standard 130 nm CMOS process and occupies an active area of 0.1 mm^2.**

I. Introduction

The Gilbert-cell is one of the most widely used active mixer designs because its double balanced structure produces excellent port-to-port isolation, it provides good conversion gain and it is convenient for monolithic implementation. The advantages of the Gilbert cell must be taken in the context of its power consumption and lower third-order intercept point (IP3) relative to passive mixers.

While linearization techniques to reduce intermodulation distortion (IMD) in amplifiers are plentiful [1]–[6], linearization methods for active mixers are fewer but they do exist. In [7], [8], for example, distortion cancellation in Gilbert-type mixers using the method of derivative superposition (DS) was employed with promising results. The fundamental idea behind DS is to use auxiliary transistors biased near pinchoff so that that they produce strong IMD tones that are out of phase relative to the IMD tones of the main circuit. Hence, when the IMD tones of the main circuit and the auxiliary devices are summed they cancel out [9].

This paper reports an active downconverter mixer that uses DS to improve the IIP3 of the circuit. Measurements on the mixer with the auxiliary transistors turned on show that its IIP3 is 14 dB higher compared to when the auxiliary devices are off. The distortion-cancelling mixer operates at an RF frequency of 1 GHz and has a conversion gain of 11 dB. The chip was fabricated using IBM's standard 0.13-μm CMOS process.

II. Distortion-Cancelling Mixer

Fig. 1 shows the proposed mixer circuit. The dotted box contains the mixer core while the auxiliary transistors used for distortion-cancellation are outside the box. Since the dominant contributor to IMD in Gilbert-cell mixers comes from the RF stage [10], the auxiliary transistors, M_{1a} and M_{2a} are placed in parallel with the RF transconductor devices, M_1 and M_2. The mixer core is a typical double-balanced Gilbert cell mixer with resistive loads. The drain terminals of the auxiliary devices are capacitively coupled to the mixer core through large capacitors. Transistors M_5 and M_6 serve as the current source for the auxiliary transistors.

Compared with previous works [7], [8] where the DS circuit is embedded inside the mixer and shares the dc bias current with the mixer core, in this paper the DS circuit is biased independently from the core. As a result, the mixer's conversion gain is minimally affected with the addition of the distortion-cancelling circuitry. Furthermore, the proposed topology also minimizes the distortion produced by second-order transconductance g_{m2} and by harmonic feedback [11].

To illustrate how distortion cancellation occurs in the proposed mixer, consider the small-signal drain current, i_{d1}, of M_1 in Fig. 1 when the device is biased in saturation. That current be written as the polynomial series

$$i_{d1}(v_{gs}) = g_{m1,1}v_{gs} + g_{m2,1}v_{gs}^2 + g_{m3,1}v_{gs}^3 + \cdots \quad (1)$$

where $g_{mn,1}$ is the n^{th}-order small signal transconductance of M_1. A similar expression applies to the drain current of M_2 It is well-known that the $g_{mn,1}$ terms have

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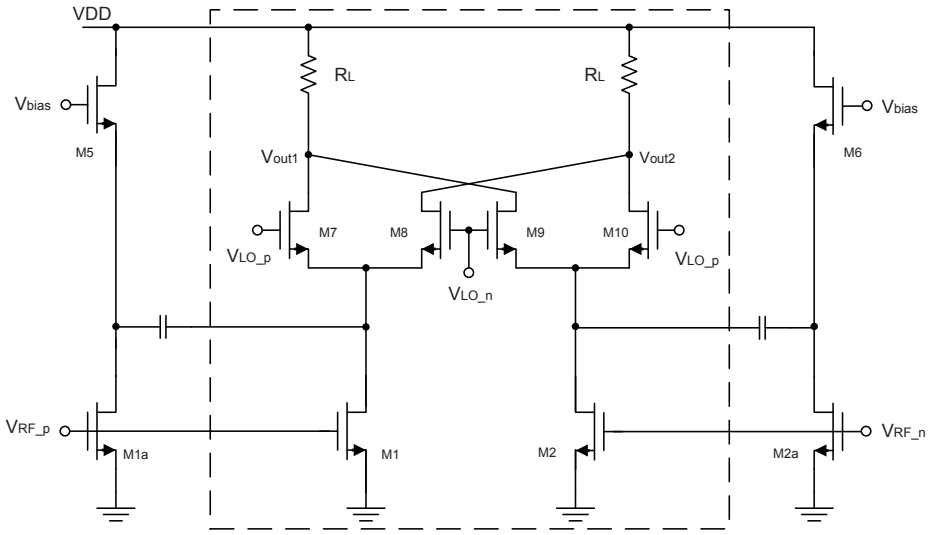

Fig. 1. The proposed distortion-cancelling downconverter mixer. Simplified biasing arrangement shown.

a strong dependence on the dc gate-to-source voltage V_{GS} of the transistor and that dependence can be written as

$$g_{m1,1}(V_{GS}) = \frac{\partial I_D}{\partial V_{GS}} \tag{2}$$

$$g_{m2,1}(V_{GS}) = \frac{1}{2}\frac{\partial^2 I_D}{\partial^2 V_{GS}} \tag{3}$$

$$g_{m3,1}(V_{GS}) = \frac{1}{6}\frac{\partial^3 I_D}{\partial^3 V_{GS}} \tag{4}$$

It is useful to have an equation that predicts the IIP_3 of the circuit based on the nonlinear transconductance terms. Such equation exists and is given by [3]

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{g_{m1,1}}{g_{m3,1}}\right|}. \tag{5}$$

If the input impedance is matched to 50 Ω, the IIP3 can be written in dBm as:

$$IIP3 = 10\,\log\left(\frac{40}{3}\left|\frac{g_{m1,1}}{g_{m3,1}}\right|\right). \tag{6}$$

In the DS technique, the $g_{m3,1}$ of M_1 is reduced by placing an auxiliary transistor, M_{1a}, in parallel with M_1 as shown in Fig. 2. The dc gate bias voltages of M_1 and M_{1a} are selected such that their third-order transcondcutances satisfy the relationship: $g_{m3,1a} = -g_{m3,1}$. In this manner, the third-order distortion terms in i_{d1} and i_{d1a} disappear from the output current, I_{out}, when they are added at top node.

Since transistor M_1 is in saturation, its $g_{m3,1} < 0$ and, thus, the auxiliary device has to be biased in weak inversion where its $g_{m3,1a} > 0$. To verify this claim, the $g_{m3,1}$ of M_1 was found as a function of V_{GS} through

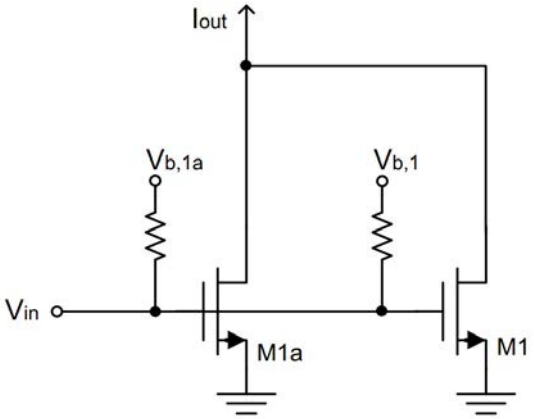

Fig. 2. Illustration of the DS technique using two FET's.

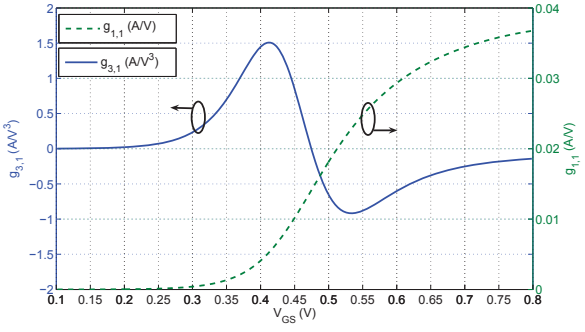

Fig. 3. Behavior of the $g_{m1,1}$ and $g_{m3,1}$ transconductance terms of transistor M_1 as a function of its V_{GS} bias voltage.

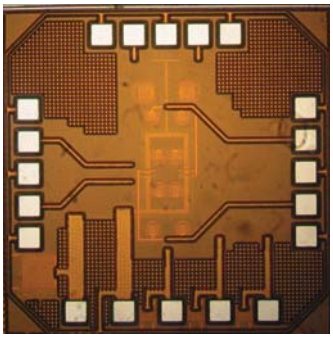

Fig. 4. Microphotograph of the distortion-cancelling mixer chip.

simulation and the results are plotted in Fig. 3. In the simulation, V_{DS} was set to 360 mV and the the transistor dimensions were L = 0.13 μm and W = 60 μm. The plot shows that for $V_{GS} < 0.47$ V (weak inversion), $g_{m3,1}$ is positive and for $V_{GS} > 0.47$ V (strong inversion) $g_{m3,1}$ is negative. The foregoing discussion applies as well to the transistor M_2 in Fig. 1 and its auxiliary transistor M_{2a}.

III. Experimental Results

The mixer chip was fabricated using IBM's 130 nm CMOS process. The RFIC occupies a die area of 0.2 mm $\times$ 0.5 mm without bonding pads and 1 mm $\times$ 1 mm with bonding pads. A microphotograph of the chip is shown in Fig. 4. Coplanar GSGSG differential probes were used to test the chip. Wideband off-chip baluns were used at the RF and LO ports to generate the required differential input signals. At the IF port, a unity-gain off-chip buffer was used to convert the signal from differential to single-ended and for impedance matching between the chip and the test equipment.

The mixer's conversion gain and IIP_3 were first measured with the distortion-cancelling auxiliary devices turned off to get the baseline performance of the mixer. To turn off the auxiliary devices the bias voltages $V_{GS,1a}$ and V_{bias} in Fig. 1 were both set to 0 V.

The conversion gain of the baseline mixer was measured at 11.7 dB for an RF input frequency of 1 GHz and an LO frequency of 800 MHz. Fig. 5 shows a plot of the baseline mixer's conversion gain versus RF input power. The $\text{IP}_{1\text{dB}}$ of the mixer is around -15 dBm, from which the $\text{OP}_{1\text{dB}}$ is easily inferred to be -3.3 dBm. When the distortion-cancelling transistors are turned on, the mixer's conversion gain (not shown in the graph) drops slightly to 11 dB while its $\text{IP}_{1\text{dB}}$ remains constant.

Two-tone tests were carried out on the mixer to determine its IP_3. The RF input tone frequencies were set to 1000.5 MHz and 999.5 MHz and the LO frequency was again set to 800 MHz. Figs. 6 and 7 show the two-tone

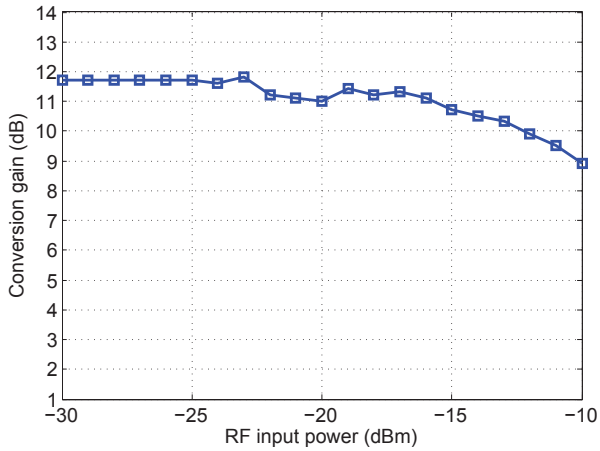

Fig. 5. Measured conversion gain of the baseline mixer vs. RF input power at 1 GHz.

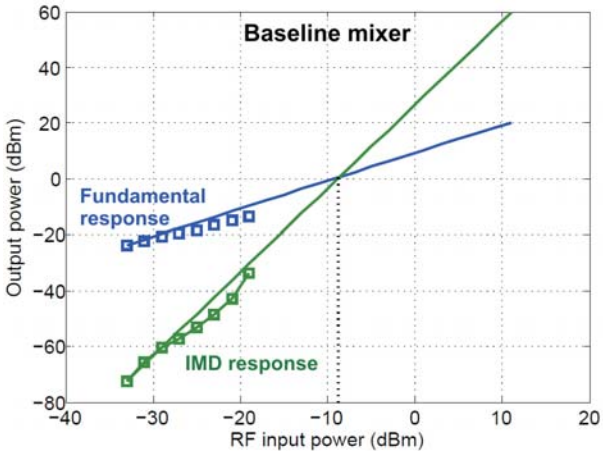

Fig. 6. Measured two-tone test results of the baseline mixer.

test results of the baseline and distortion-cancelling mixers, respectively. We observe that the baseline mixer has an IIP_3 of -9 dBm while the distortion-cancelling mixer's IIP_3 is +14 dB higher, at $+5$ dBm.

The two-tone test plots exhibit a frequently observed phenomenon: as the input power incrases the slope of the IMD curve deviates from 3:1. The reason for this is simple: it is because the nonlinearities that produce the IMD tones start to be dominated by the fifth and higher odd-odder distortion terms.

The port-to-port isolations of the linearized mixer were measured. The RF-to-IF isolation was approximately 50 dB and the LO-to-IF isolation was approximately 40 dB. The LO-to-RF isolation, which is important in direct conversion receivers (DCRs) and low IF receivers, was better than 72 dB.

To check the noise degradation (ND) introduced by the linearization circuit, a noise figure (NF) measurement was

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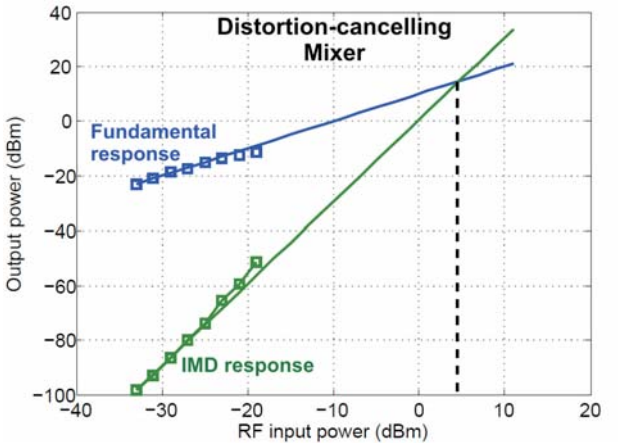

Fig. 7. Measured two-tone test results of the distortion-cancelling mixer.

TABLE I
SUMMARY OF RESULTS

Metric/parameter	value	units	
RF frequency	1.0	GHz	
LO frequency	0.8	GHz	
Chip core area	0.1	mm^2	
CMOS node	130	nm	
IIP_3	-9	dBm	baseline mixer
	5	dBm	dist. cancelling mixer
	+14	dB	change
Conversion gain	11.7	dB	baseline mixer
	11	dB	dist. cancelling mixer
	-0.7	dB	change
DC power consumption	18	mW	baseline mixer
	20.4	mW	dist. cancelling mixer
	+2.4	mW	change

performed. The results show that the single sideband noise figure (SSB NF) of the baseline mixer is 15.9 dB while the SSB NF of the distortion-cancelling mixer was roughly the same. In other words, the linearization circuit had a negligible effect on the NF of the mixer.

The baseline mixer draws 15 mA of dc current from a 1.2 V supply while the distortion-cancelling mixer draws 17 mA from the same 1.2 V supply. Therefore, the distortion-cancelling mixer requires an additional 2.4 mW of dc power, or 13% more, relative to the baseline mixer. A summary of the performance of the chip is presented in Table I.

IV. CONCLUSION

The derivative superposition (DS) technique has been shown to increase the linearity of an active downconverter mixer by 14 dB. Unlike the conventional DS technique where the DS circuit is embedded in the mixer circuit itself, in the proposed circuit capacitive coupling between the DS circuit and the mixer transconductor is used. This allows one to linearize a pre-existing mixer design without changing its bias conditions.

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