A 19-26 GHz Balanced Amplifier in 130 nm CMOS Technology

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***Abstract*—The design of a fully integrated balanced amplifier implemented in a 130 nm CMOS technology is described in this paper. This balanced amplifier achieves a gain of 30 dB from 19 GHz to 26 GHz. To reduce the signal loss and the physical dimensions of the 90° coupler utilized in this balanced amplifier, a meandered broadside coupler with shield is designed. This on-chip 90° coupler occupies a compact area of 300 um x 120 um. An effective technique based on tuning the width of the transistors to achieve wideband operation is also proposed in this paper. The proposed balanced amplifier design achieves an IIP_3 of -6.0 dBm and an input 1-dB gain compression point of -16.5 dBm. The OIP_3 and the output 1-dB gain compression point are 24.0 dBm and 10.7 dBm, respectively.**

Keywords- Balanced amplifier; wideband amplifier; K-band; microwave components; on-chip 90° coupler; CMOS

I. Introduction

The balanced amplifier circuit, shown in Figure 1, is a practical way to implement amplifiers for wireless communications system at very high RF frequencies [1] with good input and output matching, a high degree of stability, and high linearity. Its basic topology has not changed much since its first introduction in a hybrid form [2]. Since then, numerous works have been devoted to implement this topology in monolithic form [3] [5]. Only until recently however, has a balanced amplifier been demonstrated in a CMOS technology, which was a narrowband design at 45 GHz [4].

The physical sizes of the balanced amplifier at K-band (19-26 GHz), where it is utilized for broadband network consumer applications such as automotive radars and satellite communications, have particularly caused difficulties for realization and integration in a commercial CMOS process. One of the major issues associated with implementing the balanced amplifier at K-band in CMOS technology arises from the large physical dimension of the required 90° coupler, and the poor coupling ratio due to signal loss in the relatively low-resistivity CMOS substrate. As a numerical example, the length of a single section K-band 90° coupler is around 1.6 mm in a SiO_2 dielectric medium. To solve these issues, a meandered broadside coupler with broadside shield is designed and presented in Section III of this paper.

To date, previous researches have demonstrated narrowband balanced amplifiers in CMOS technology [4] [9]. However, a broadband balanced amplifier that fully utilizes the broadband operation of the 90° coupler has been difficult to achieve in CMOS technology. In Section IV of this paper, an effective technique based on tuning the widths of the transistors to achieve wideband operation is described.

II. System Overview

Figure 1 illustrates the system topology of the balanced amplifier circuit. It consists of two identical amplifier modules terminated in parallel with one 3-dB, 90° coupler at the input and one at the output. A signal is first split between port 2 and 3 of the 3-dB Coupler I with a 90° phase shift at port 3. These two split signals are then independently amplified by Amplifier I and II, which introduce a phase shift of θ_{amp} on both amplified signals. Coupler II provides an additional 90° phase shift and combines these two amplified signals at port 2 and 3. The combined amplified signal is obtained at the output port of Coupler II.

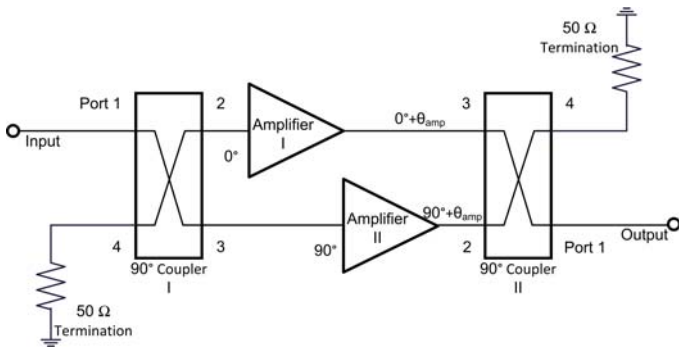

Fig. 1. A simplified balanced amplifier circuit topology

Suppose the 90° couplers are characterized by S-parameter matrices, s^c_{jk}, where j and k are the corresponding port number, and the amplifiers are characterized by their corresponding 2-port S-parameter matrices, s^{ampi}, with the isolated port 4 terminated with matching impedance, through derivation, it is seen that the S-parameter matrix of the overall system, S_{BA}, becomes

$$\begin{pmatrix} \left(s^c_{12}\right)^2 s^{amp1}_{11} + \left(s^c_{13}\right)^2 s^{amp2}_{11} & \left(s^{amp1}_{12} + s^{amp2}_{12}\right) s^c_{12} s^c_{13} \\ \left(s^{amp1}_{21} + s^{amp2}_{21}\right) s^c_{12} s^c_{13} & \left(s^c_{12}\right)^2 s^{amp2}_{22} + \left(s^c_{13}\right)^2 s^{amp2}_{22} \end{pmatrix}. \quad (1)$$

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With a further assumption of ideal 3-dB 90° coupling, i.e. $s_{12}^c = \frac{j}{\sqrt{2}}, s_{13}^c = \frac{-1}{\sqrt{2}}$, and the 2-port S-parameters of the two amplifier modules are identical, i.e., $s^{amp1} = s^{amp2}$, the S-parameter matrix of the balanced amplifier simplifies to

$$S_{BA} = \begin{pmatrix} 0 & -js_{12}^{amp} \\ -js_{21}^{amp} & 0 \end{pmatrix}$$

which verifies the functionality of the balanced amplifier topology [1], i.e., providing signal gain at the level of the amplifier module (having the same magnitude of the transmission and the reverse isolation coefficients as the amplifier module) with excellent input and output matching with the aid of the 90° couplers (having ideal reflection coefficients of zero).

In the next section, the physical implementation of the 90° couplers is described in detail. Namely, a meandered broadside coupler with broadside shield is designed to solve the physical dimension and the signal loss issues.

III. Meandered Broadside Coupler with Broadside Shield

Miniaturization of passive circuit components has always been a key topic of monolithic system integration for CMOS RF integrated circuits. Since the dimensions of any passive circuit are dependent on the signal wavelength, the physical sizes of these passive structures in CMOS technology can lead to prohibitively large and expensive ICs. To overcome this design challenge, two main techniques have been proposed. One is aggressive transmission-line meandering [6], which achieves minimization of the physical dimensions through modification of the planar geometry, and the other is multilayered design techniques incorporating slow-wave structures [7] [9]. At the same time, due to the lossy silicon substrate of a standard CMOS technology, effective shielding of the signal lines from the substrate is necessary. In addition, the ever stringent metal density requirements need also be taken into account for manufacturing yield purpose as well.

To address these issues, we propose a 3-dB 90° coupler design using a 130 nm CMOS technology, which has eight metal-layers M1-M8. This 3-dB 90° coupler design utilizes the aggressive meandering technique to shrink the physical dimension from a potential 1600 um x 25 um to a much more practical and compact 300 um x 120 um. Simultaneously, we exploit the tightly stacked CMOS metal layers [10] to construct a pair of ground shielding layers that ensure the signals travel through the strip conducting lines of the coupler in TEM mode, and shield the signals from potential loss to the lossy silicon substrate. Figure 2 illustrates the cross section of the proposed meandered broadside 90° coupler with broadside shield.

Since the capacitance between the coupling lines is a function of the physical dimension, to better control the geometry, metal layers M4 and M5 of the eight metal-layer CMOS technology are employed for the strip conducting lines, as they are approximately in equal distance to the ground shielding planes on metal layers M2 and M6. Material-wise, these two layers are made of copper as opposed to aluminum; hence they

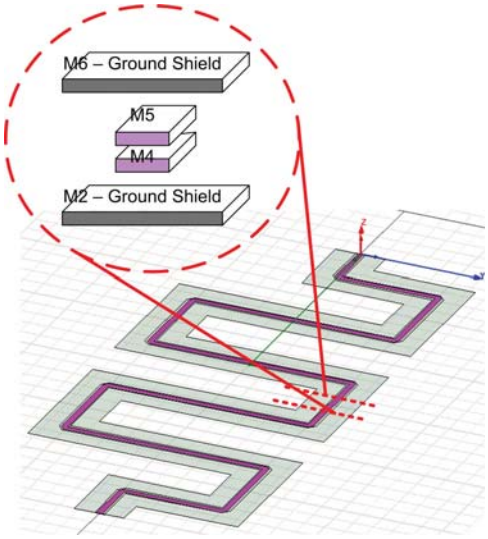

Fig. 2. Cross section with an aerial view of the proposed broadside coupler with broadside shield

further reduce potential signal loss since copper has higher conductivity. The broadside shields on metal layers M2 and M6 ensure the signals travel through the strip conducting lines in TEM mode, and shield the signals from potential loss to the lossy Silicon substrate. Furthermore, since the two topmost metal layers (M7 and M8) of the eight-metal-layers process [10] are still unused and are being shielded from the coupler by the broadside shield on metal layer M6, they can be filled with dummy metals to meet the metal density requirements for manufacturing purposes. The equalization of characteristic impedance of each coupled line is performed through iterative optimization of the line width from EM simulation results. Based on EM simulations, the widths of the metal layers for the 3-dB 90° broadside coupler with broadside shield are designed to be 25 um, 5 um, 3 um, and 25 um, for metal layer M2, M4, M5, and M6, respectively.

A. EM Simulation Results

The Momentum EM simulation [11] results of this design are shown in Figure 3. Over a wide frequency range from 18 GHz to 33 GHz, the insertion loss of s_{21} and s_{31} on average is approximately 3.5 dB, and the phase difference between the two ports is approximately 95°. At the same time, the input and output reflection coefficients s_{11} and s_{33} are better than -20 dB across the entire operating range. Since the insertion loss of s_{21} and s_{31} varies from 3 dB and the phase difference between the two ports deviates from 90°, the effect of these component nonidealities on the reflection coefficients of the balanced amplifier is further investigated based on equation (1). The normalized effect on the input and output reflection coefficients (defined as $(s_{12}^c)^2 + (s_{13}^c)^2$, which is the ratio of the reflection coefficients of the balanced amplifier to the reflection coefficients of its amplifier module) is illustrated in Figure 4. This investigation reveals that for the balanced amplifier, the phase difference variation of the coupler is the

main cause of the input and output reflection coefficients degradation from its ideal scenario. To ensure good input and output reflection coefficients for the balanced amplifier, the 90° coupler is designed with less than 10° phase difference variation between the port 2 and 3.

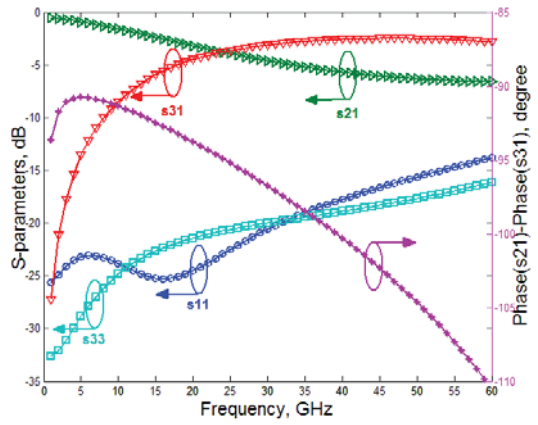

Fig. 3. S-parameter response of the broadside coupler with broadside shield

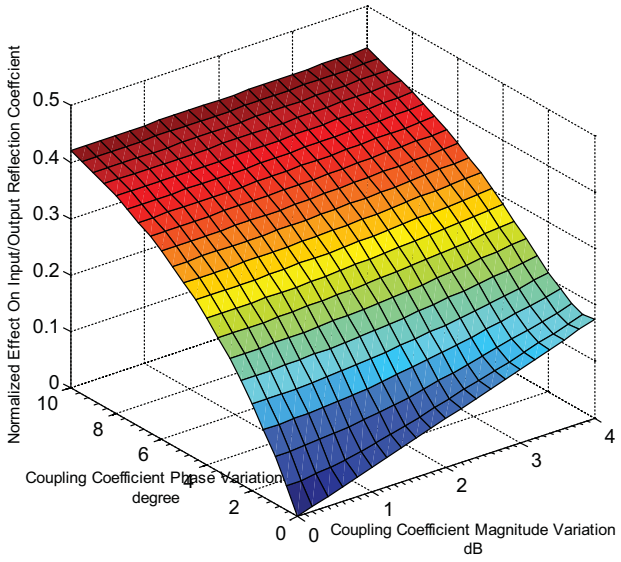

Fig. 4. The effect of the insertion loss and the phase variation of the 90° coupler on the input and output reflection coefficients of the balanced amplifier

IV. Amplifier Module Design

Figure 5 illustrates the amplifier module. In the frequency range of interest, i.e., 19-26 GHz, the parasitic capacitance C_{GS} of each transistor is the major limitation to fully utilize the small-signal gain of the common-source circuit topology. To overcome this limitation, inductors (shown as L_{SHUNT}) are utilized to form parallel resonators with these parasitic capacitances at the operating frequency. These inductors in effect resonate out the parasitic capacitances at the frequency of operation [4] [8] [9]. However, this traditional approach also limits the operating bandwidth.

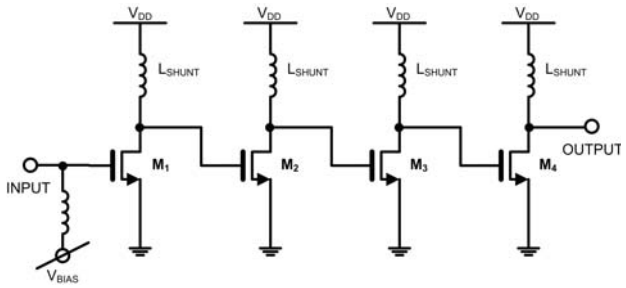

Fig. 5. Amplifier module of the balanced amplifier circuit topology

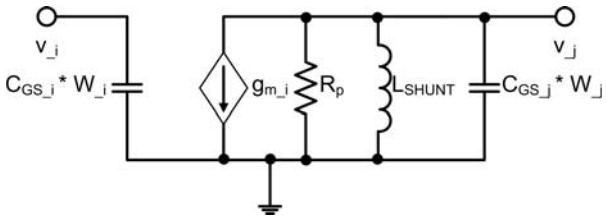

Fig. 6. Small signal model of the common-source circuit with shunting inductor L_{SHUNT}

To mitigate this situation, the width of each transistor in the common-source configuration is introduced as an additional design variable. Figure 6 illustrates the simplified small signal equivalent model of one common-source subsection of the amplifier module. From this small signal model, the voltage gain of each common-source amplifier *i* can be expressed as follows,

$$A_{v_i}(s) = \frac{s\frac{g_{m_i}}{C_{GS}*W_j}}{s^2 + s\frac{1}{R*C_{GS}*W_j} + \frac{1}{C_{GS}*W_j*L_{SHUNT}}}. \quad (2)$$

Here g_{m_i}, W_i, and C_{GS} are the transconductance, the width and the gate-oxide capacitance per unit width of transistor *i* (*j* is the subsequent transistor). L_{SHUNT} is the inductor that is used to resonate out the nominal parasitic capacitance at the frequency of operation. R is the resistance seen at node v_j.

With the width of the transistor as the additional design variable, each small signal gain expression of the common-source amplifier adduce to a band pass response with two distinct poles at,

$$s_{1,2} = \frac{-L_{SHUNT} \pm \sqrt{L_{SHUNT}^2 - 4R^2C_{GS}W_jL_{SHUNT}}}{2RC_{GS}W_jL_{SHUNT}}. \quad (3)$$

Each common-source amplifier, as a sub-section of the amplifier module, contributes a pair of conjugate poles for a band-pass response. With these four common-source amplifiers cascaded, a total of eight poles are formed, which are supplied by eight coupled nonlinear design equations. A numerical iterative optimization programming is used to compute the values of the four design variables, i.e., $W_1 = 56um, W_2 = 36um, W_3 = 92um$, and $W_4 = 56um$, such that the overall amplifier module achieves a broadband band-pass response from 17 GHz to 30 GHz.

V. Simulation Results

The balanced amplifier has been designed and simulated with parasitic-extracted netlist in IBM's 130 nm RF CMOS process with V_{DD} = 1.2 V. Figure 7 shows the simulated S-parameters and the noise figure (NF) of the fully integrated balanced amplifier. A forward gain of 30 dB is achieved with 3 dB bandwidth from 19 GHz to 26 GHz. The reverse isolation is around -40 dB across the operating bandwidth. Figure 7 also shows that both the input reflection coefficient s_{11} and the output reflection coefficient s_{22} achieving better than -12 dB across the operating bandwidth. In addition, the simulated noise figure varies from 7.5 dB to 11 dB across the operating bandwidth.

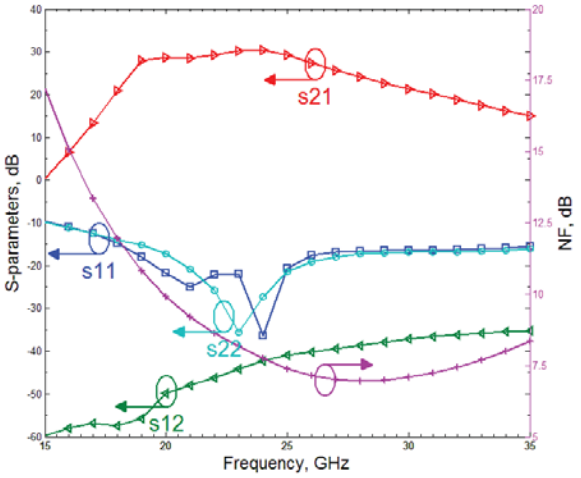

Fig. 7. S-parameters and NF of the balanced amplifier

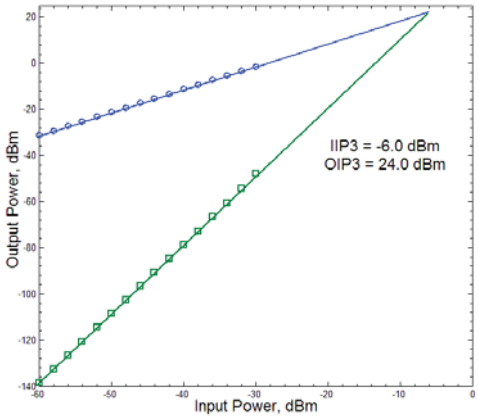

Fig. 8. Linearity measurement of the balanced amplifier at 24 GHz

The balanced amplifier has an IIP_3 of -6.0 dBm at 24 GHz with 10 MHz adjacent channel spacing (Figure 8). Its input 1-dB gain compression point at 24 GHz is -16.5 dBm. The OIP_3 and the output 1-dB gain compression point are 24.0 dBm and 10.7 dBm, respectively. In addition, a maximum output power of 11.5 dBm is obtained with a small signal gain of 30.0 dB (Figure 9). The circuit draws 144 mW of power from a 1.2 V power supply, which corresponds to a peak drain efficiency of 9.8%.

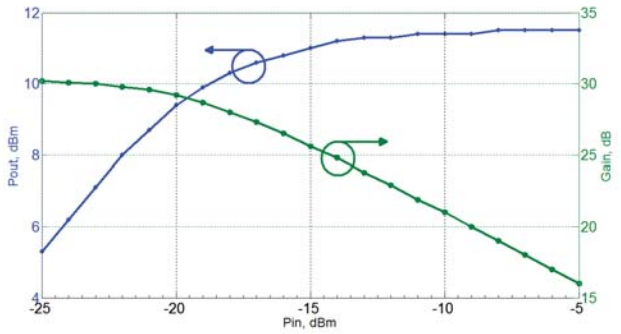

Fig. 9. Output power and amplifier gain vs. available input power at 24 GHz

VI. Conclusion

A fully integrated balanced amplifier has been designed and simulated in IBM 130 nm RF CMOS process. A 30 dB gain with a wideband bandwidth from 19 GHz to 26 GHz is obtained with 144 mW of power dissipated from a 1.2 V supply. This work demonstrated a fully integrated broadband balanced amplifier at K-band that would be implemented in a low-cost CMOS process. A comparison of similar works with this work is summarized in Table I.

	This Work	[4]	[12]	[13]	[14]
Process	0.13 um CMOS	0.18 um CMOS	0.18 um CMOS	0.1 um InGaAs/AlGaAs/ GaAs HEMPT	0.18um CMOS
Gain, dB	30.0	21.5	45.0	17.0	7.0
Operating frequency, GHz	19-26	45.4	23.7	9-20.0	22.9-26.0
S11, dB	-15.0	-13.0	-10.8	-12.0	-12.0
S22, dB	-15.0	-14.9	-9.1	-15.0	-20.0
NF, dB	11.0	12.8	10.8	2.3	-
$P_{1dB,out}$, dBm	10.7	-	-2.3	15.0	13.0
P_{maxout}, dBm	11.5	-	3.0	16.0	14.5
Broadband	Yes	No	No	Yes	No
Power, mW	144.0	89.0	123.0	188.0	280.0

Table I. Summary of comparison

Acknowledgment

The authors thank Natural Sciences and Engineering Research Council of Canada for providing funding support, and Dr. Al Freundorfer for providing insightful technical discussions.

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