Fully Monolithic Single-Sideband Upconverter Mixer with Sideband Selection

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***Abstract*—A single-sideband upconverter mixer with sideband selection capability is presented. Sideband selection is accomplished by inverting the polarity of either the I or Q differential IF signals into the upconverter by means of a switch network. The mixer operates at an LO frequency of 5 GHz and an IF of 100 MHz, and thus it produces an upper sideband at 5.1 GHz and a lower sideband at 4.9 GHz. Experimental results show that the mixer has a conversion gain of over 12 dB and that its IP_{1dB} is -12 dBm and its IIP3 is -5 dBm. The OP_{1dB} and OIP3 of the upconverter are 0 dBm and +6.5 dBm, respectively. The chip was fabricated using a standard 130 nm CMOS process, it consumes a total of 26 mW of dc power and the circuit core occupies an area of 0.49 mm^2.**

***Index Terms*—upconverter, mixer, single sideband, image rejection, RFIC, CMOS**

I. Introduction

Single-sideband (SSB) upconverters, even fully monolithic ones, have often used distributed passive circuits to generate the I/Q signals needed in the mixing core, inevitably requiring a large die area. However, by using lumped-element power couplers and novel phase shifting techniques, the die area of an SSB upconverter can be reduced [1], [2], [3]. A common design tradeoff in choosing a lumped-element circuit over a distributed one for I/Q signal generation is between die area and phase balance, which has a direct impact on the amount of sideband rejection of the mixer [4], [5].

An SSB upconverter is described in this paper which can produce either the upper sideband (USB) or the lower sideband (LSB) by toggling a dc control voltage. To the best of the author's knowledge, this is the first monolithic implementation of an SSB upconverter mixer with an internal band selection mechanism. The sideband selection is implemented by inverting the polarity of either the I or Q differential IF signals into the mixing core by applying the control voltage to a switch network. The ability to select the sideband in the upconverter makes this circuit suitable for reconfigurable radios. The upconverter exhibits a conversion gain of over 12 dB and has an IP_{1dB} of -12 dBm. Furthermore, the upconverter has an IIP3 of -5 dBm and an OPI3 of 6 dBm. The measured sideband rejection greater than 30 dB when the chip is operating in either the USB or the LSB mode.

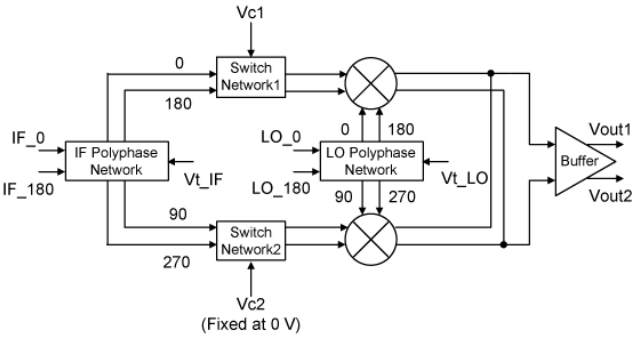

Fig. 1. Proposed SSB upconverter with sideband selection

II. SSB Upconverter Design

A block diagram of the SSB mixer with sideband selection is depicted in Fig. 1. It consists of five components: an IF polyphase network, an LO polyphase network, two switch networks, the mixing core, and an on-chip RF output buffer.

The RC polyphase networks [4] convert the differential IF and LO input signals into quadrature signals which are fed to the mixing circuits. Transistors biased in triode were employed as variable resistors in the polyphase networks in order to optimize the phase balance of the output signals at the frequencies of interest. A circuit diagram of the IF polyphase network is shown in Fig. 2. Since the IF frequency is at 100 MHz, the MOS transistors would need to produce a resistance of 330 Ω if a 5 pF capacitor is used, for example. This is a large value of resistance relative to what is possible with a short-channel MOS device and therefore a fixed resistor, R, of 280 Ω was added in series with the transistors. This was a reasonable compromise because it allowed for a compact design while providing a useful amount of I/Q phase tuning at the same time. The LO polyphase network was nearly identical to the IF network, except that the fixed resistors in Fig. 2 were not used because the LO frequency was sufficiently high at 5 GHz so that the MOS devices were able to provide the required resistance by themselves.

The mixing core of the SSB upconverter is re-drawn in Fig. 3. It is the Hartley SSB mixer configuration [6], [7] and we can easily show that the output currents are: $I_{out1,2} = \pm\, I\cos(\omega_{LO}t + \omega_{IF}t)$, which is the upper sideband. Now, if the polarity of the IF_I signals into the top mixer in Fig. 3 are

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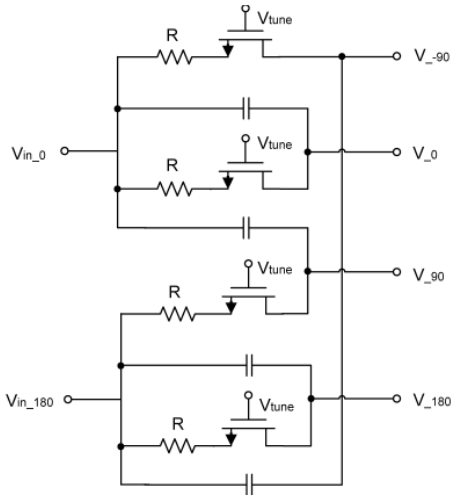

Fig. 2. IF polyphase network

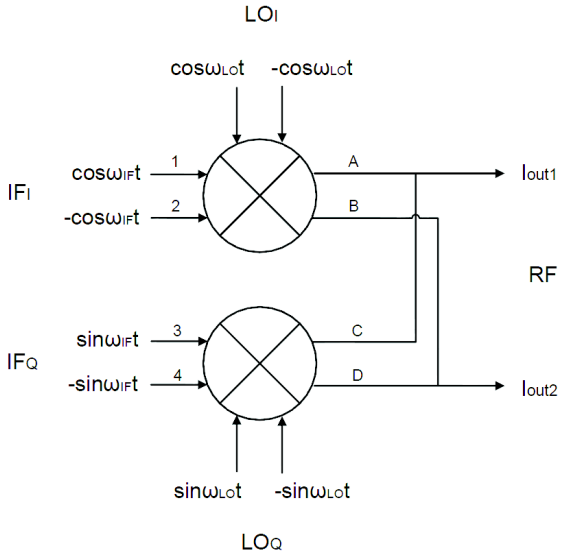

Fig. 3. Close-up view of the mixing core of the SSB upconverter

inverted, then the lower sideband is generated and the output currents are given by $I_{out1,2} = \pm\, I\cos(\omega_{LO}t - \omega_{IF}t)$. Note that the same result is obtained if the IF_Q signal polarities are inverted instead.

The function of the switch network in Fig. 1 is to invert the polarity of the differential input signals of either the IF_I or IF_Q paths. Fig. 4 shows the switch network used in this design, where V_c is the applied control voltage and $\overline{V_c}$ is generated from V_c using a digital inverter. When the control voltage V_c is high (1.2 V) and is low (0 V), the output signals are $V_{out1} = V_{in1}$ and $V_{out2} = V_{in2}$. On the other hand, when the control voltage V_c is low, the output signals would be $V'_{out1} = V_{in2}$ and $V'_{out2} = V_{in1}$. In this manner we can invert the polarity of the differential input signals.

The transistors in the switch network had a moderate gate width of 20 μm in order to keep the parasitic capacitances at a reasonably low level and the series ON resistance small.

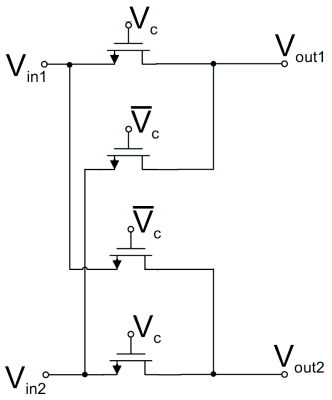

Fig. 4. The switch network used for signal polarity inversion

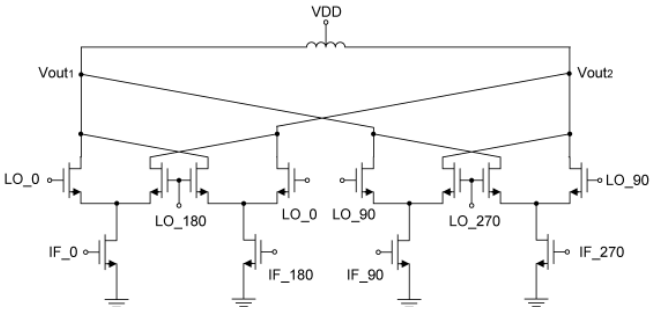

Fig. 5. The mixer core with inductor load

Simulations reveal that the switch network has an insertion loss of 0.2 dB. Referring to Fig. 1, when V_{c1} equals 0 V, the upper sideband is selected while the lower sideband is suppressed. Conversely, when V_{c1} equals 1.2 V, the lower sideband is selected instead while the upper sideband is suppressed.

While it is only necessary to change the polarity of either IF_I or the IF_Q signals and only one switch network could be used, two switch networks are included in this design in order to provide an equal loading to the IF polyphase network. This helps to ensure that the IF signals entering the mixer will have the same amplitude and phase balance.

Two interconnected Gilbert multiplier cells were used as the mixing core of the upconverter. The circuit is shown in Fig. 5. An inductive load was used in order to provide a good amount of conversion gain while avoiding a DC voltage drop across the load. The inductor was a parallel-stacked spiral inductor with a ground plane beneath in order to maximize the inductor's quality factor [8]. The mixing core has a simulated conversion gain of about 15 dB.

III. Experimental Results

The IF and LO frequencies chosen for the testing of the SSB upconverter were 100 MHz and 5 GHz, respectively, resulting in an USB of 5.1 GHz and a LSB of 4.9 GHz.

A spectral measurement of the upconverter mixer when it is in USB mode is shown in Fig. 6. From the spectral

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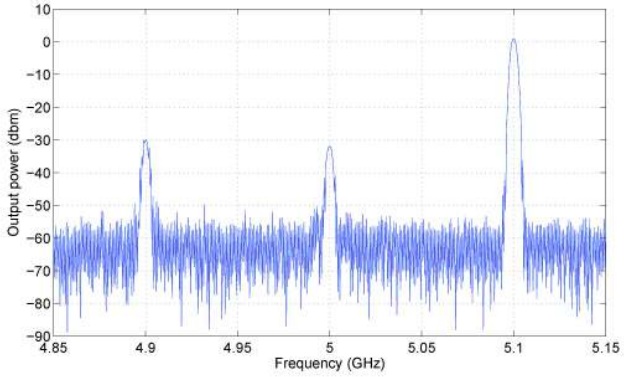

Fig. 6. Measured output spectrum of the mixer in USB mode

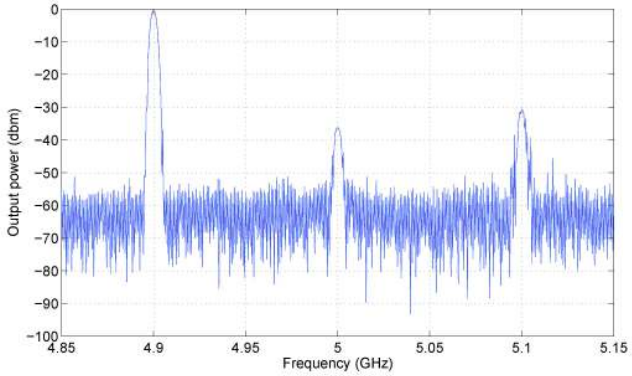

Fig. 7. Measured output spectrum of the mixer in LSB mode

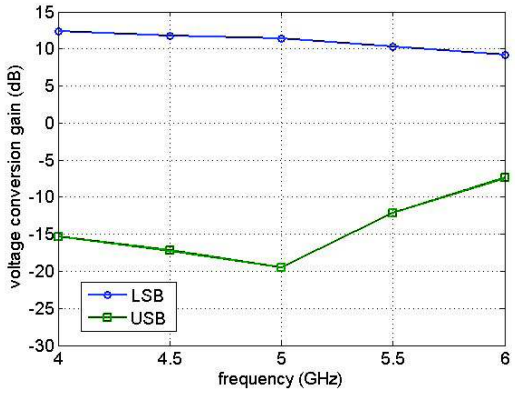

Fig. 8. Frequency response of the mixer in LSB mode.

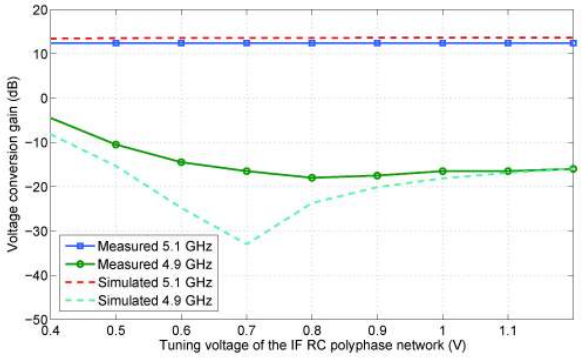

Fig. 9. Mixer conversion gain as a function of the IF polyphase network tuning voltage when the mixer is in USB mode.

measurement, the power of the output signal at 5.1 GHz is approximately 0 dBm while the LSB signal is approximately 30.4 dB relative to the USB tone.

The spectral output of the upconverter mixer operating in LSB mode is shown in Fig. 7. In this case, the switch network control voltage was set to 1.2 V. The power of the 4.9 GHz tone was 0 dBm and the rejection of the USB was 31 dB. Fig. 8 shows the frequency response of the mixer's voltage conversion gain when it is in LSB mode. The 3-dB bandwidth of the mixer is 2 GHz and the gain roll-off is gradual.

The amount of sideband rejection depends, amongst other factors, on the phase balance of the IF and LO input signals into the mixer core. Fig. 9 shows the measured voltage conversion gain of the mixer output signals when the circuit is operating in USB mode. The voltage conversion gain is plotted as a function of the IF polyphase network's tuning voltage. The highest LSB rejection is 30.4 dB and it is obtained when the IF tuning voltage is set to 0.8 V. Conversely, when the mixer is operating in LSB mode, the highest USB rejection is 31 dB and it also occurs when the IF tuning voltage is set to 0.8 V, as expected. The corresponding plot for the latter case is shown in Fig. 10.

The power performance of the SSB upconverter was measured in USB mode. The tuning voltages of the IF and LO phase shifter were both set to 0.8 V. The measured result is shown in Fig. 11. The IP_{1dB} is -12 dBm while the corresponding OP_{1dB} is 0 dBm. While not shown on the graph in Fig. 11, a two-tone test was also carried out and the IIP3 of this mixer is -5 dBm and its OIP3 is +6.5 dBm. Simulations show that when the upconverter is in LSB mode, similar results are obtained for the P_{1dB} and IP3 as in the measured USB mode results.

The LO-to-RF port isolation was measured and it is above

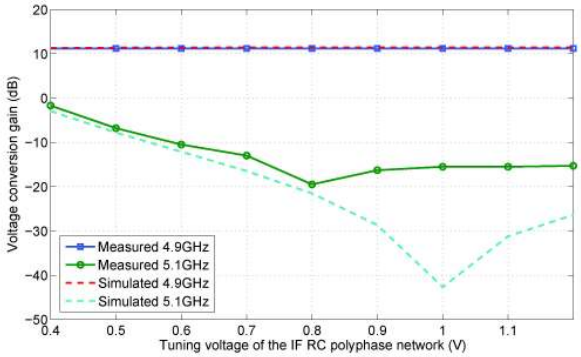

Fig. 10. Mixer conversion gain as a function of the IF polyphase network tuning voltage when the mixer is in LSB mode.

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TABLE I
SSB UPCONVERTER PERFORMANCE SUMMARY AND COMPARISON TABLE

		This Work	[1]	[2]
Technology		**130 nm CMOS**	0.15-μm pHEMT	0.35-μm SiGe
RF Frequency Band	(GHz)	**5.0**	15	2.7 & 5.4
Max. Conversion Gain	(dB)	**12.4**	18.3	0.5
Sideband Rejection	(dB)	**>30**	63	62.9
Selectable Sideband?		**Yes**	No	No
Output P_{1dB}	(dBm)	**0**	-6	-7
Output IP3	(dBm)	**6.5**	8	4
Min. LO-RF isolation	(dB)	**30**	31	24
DC Power	(mW)	**26**	86	36
Chip Area	(mm^2)	**0.49** (core)	1.26	1.0

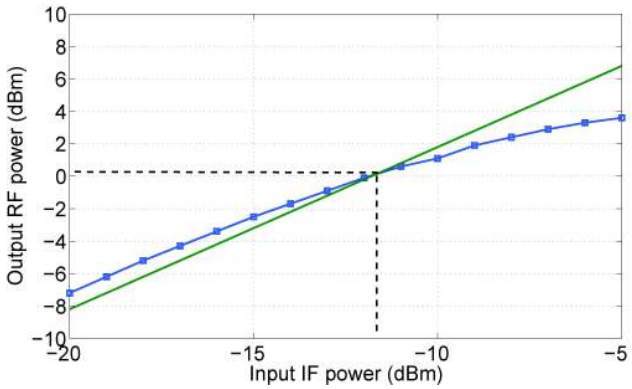

Fig. 11. Measured power performance of the upconverter

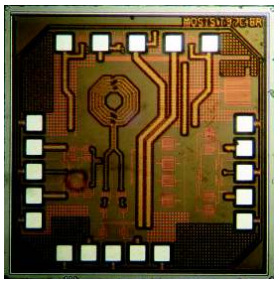

Fig. 12. Photograph of the fabricated chip

30 dB in both the USB and LSB operating modes.

The SSB upconverter was fabricated using a standard 130 nm CMOS process. It occupies a die area of 0.49 mm^2 without bonding pads and 1 mm^2 with bonding pads. Fig. 12 shows a photograph of the fabricated chip. The circuit core consumes 18 mW of dc power from a 1.2 V supply and the output buffer requires an additional 8 mW, for a total of 26 mW for the entire chip. A summary of the measured results and a comparison with other SSB upconverters is shown in Table I.

IV. CONCLUSIONS

An upconverter mixer with sideband selection has been demonstrated in a standard 130 nm CMOS process. It allows the user to choose the upper sideband or the lower sideband to be transmitted. Sideband selection is achieved by inverting the polarity of the input IF signals into the mixer core. The polarity inversion is accomplished by means of a passive switch matrix and the resulting upconverter is highly compact and consumes a low amount of power.

V. ACKNOWLEDGMENTS

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