5.4 GHz Reconfigurable Quadrature Amplitude Modulator using Very High-Speed OTAs

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***Abstract*—A new concept for a quadrature amplitude modulator operating at 5.4 GHz that can be reconfigured between 4 QAM, 16 QAM and higher modulation formats is described in this paper. Vector sum in current domain is employed here to perform the direct digital modulation function. The measured data throughput at 5.4 GHz carrier frequency was 16 Mbit/s. Experimental results show that in the 16 QAM mode, the error vector magnitude (EVM) was 6.20% and the dynamic range was from -52 dBm to -8 dBm. The chip was fabricated in 0.13-μm CMOS technology and its core occupied an area of 0.09 mm^2 due to its simple architecture. The circuit consumed 20 mA of dc current from a 1.2 V supply including the output buffer.**

I. Introduction

The efficient use of the spectrum is a highly desired characteristic in any communication system. Quadrature amplitude modulation (4-QAM or QPSK), has enjoyed an extensive use due to its simple circuitry and efficient modulation scheme. To accommodate the ever-increasing demand for fast data rates in wireless applications, systems that employ higher-order QAM modulation formats have become more widespread. Moreover, the concept of using a reconfigurable modulator that can carry out different modulation formats is attractive to advanced multi-purpose radio systems that can handle multiple communication standards.

The direct conversion modulation scheme offers considerable advantages over its conventional heterodyne quadrature modulation counterpart, such as eliminating the need for the intermediate frequency (IF) oscillator and thus the IF and radio frequency (RF) filters in the transmitter and increase the data bandwidth [1], [2]. As a result, there have been demonstrations of direct-digital QAM chips operating in the 5 GHz band for broadband wirless LAN (WLAN) applications in the past few years [3], [4].

In this paper, we report a novel modulator RFIC that can be reconfigured between 4 QAM, 16 QAM and even higher modulation formats. The core of the circuit consists of two very high-speed operational transconductance amplifiers (OTAs) and a switching network where the modulation takes place. Active balun circuits and a wideband transimpedance amplifier (TIA) are used at the input and output of the circuit, respectively, for signal conditioning purposes. The circuit operates at a carrier frequency of 5.4 GHz and measured results show a 2.33 % error magnitude error (EVM) in the 4 QAM mode and 6.20 % in 16 QAM mode. The core circuits only occupy 0.09 mm^2 chip aera and consume 13 mA DC current without the output buffer.

II. Modulator Concept and Circuit Design

The block diagram of the proposed reconfigurable QAM modulator RFIC is shown in Fig. 1. The only off-chip components are the signal generator and a 90° hybrid which provide the I/Q input signals to the chip.

The I/Q quadrature input signals are subsequently converted into four basis vectors at 0° and 180° as well as 90° and 270° by the active baluns. In this work, we will also refer to the basis vectors as the $I+$, $I-$, $Q+$, $Q-$ signals. These four signals are converted from voltages into currents using two fully differential OTAs. The four pass switches are used after the OTAs to select any two orthogonal basis vectors, which are then added together to generate the desired constellation points. The four switches are controlled by a pair of binary bits, b_0b_1, and their complements, $\bar{b_0}\bar{b_1}$. For instance, if b_0b_1=11, then the switches in the signal paths of $I+$ and $Q+$ are turned on and those two current phasors are added at node M, yielding an output current vector with a phase angle of 45°. Since the vector summation is performed in the current domain a transimpedance amplifier (TIA) is used at the output of the circuit to convert the current signals back into the voltage domain. The TIA also provides the appropriate load impedance to the OTA circuits.

If the four basis vectors have the same magnitude, then the modulator will produce a 4 QAM constellation. In order to obtain a 16 QAM constellation, then the magnitudes of the basis vectors have to be properly scaled as depicted in Fig. 2. So two additional bits, b_2b_3, are used to control the magnitudes of the basis vectors generated by the OTAs. When the bit sequence $b_0b_1b_2b_3$=1100 is applied, then vector V_1 is obtained as shown in Fig. 2 and if $b_0b_1b_2b_3$=1010 is applied, the resulting vector is V_2 and so on. It is possible to obtain even higher-order constellations beyond 16 QAM from this modulator. To achieve this, more bits would be needed to get a finer control of the bias currents of the OTAs, thus leading to a greater number of basis vector amplitudes.

Fig. 3(a) shows the schematic of the active balun used in the modulator to feed the differential voltages to OTA$_i$ and OTA$_q$. A common gate common source (CG-CS) topology is used due to its small size and low power consumption. The CG stage generates the in-phase output while the CS stage

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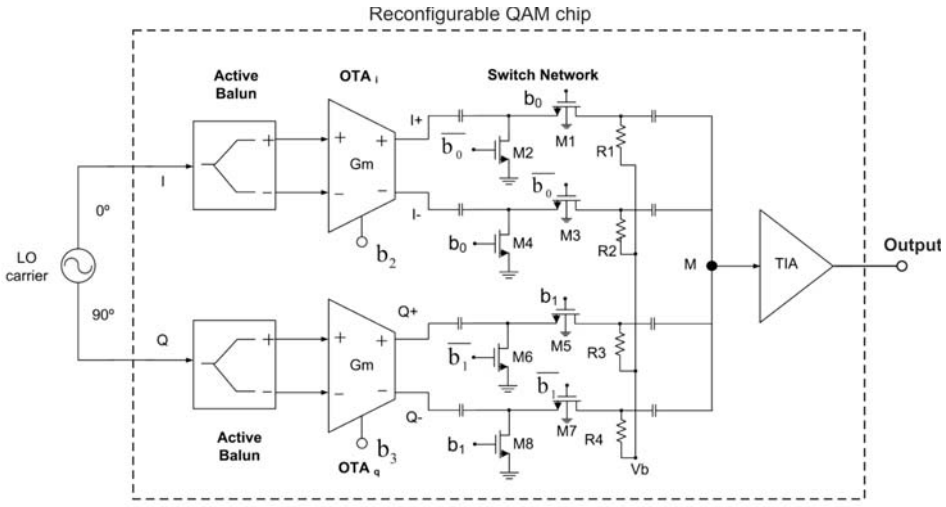


Fig. 1. Block diagram of the reconfigurable QAM modulator chip: 4 QAM (b_0b_1); 16 QAM ($b_3b_2b_1b_0$)

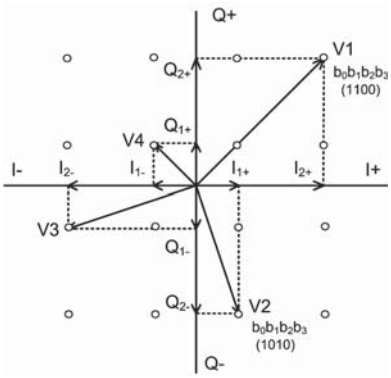


Fig. 2. Vector diagram of the proposed QAM modulator

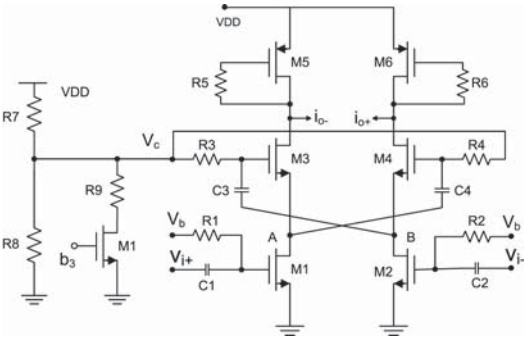
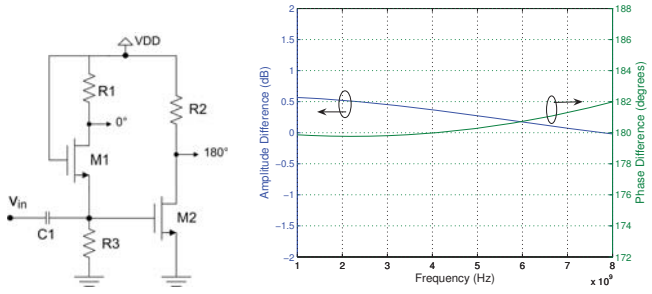


Fig. 4. Schematic of the high-speed OTA (V_b=0.6 V)



(a) (b)

Fig. 3. The schematic of the active balun (a) and magnitude/phase differences of output signals (b)

generates an output with 180° out of phase. The phase and amplitude balance of the baluns play a critical role in the overall behavior of the system because they have a direct impact on the EVM performance of the modulator. Fig. 3(b) shows the post-simulated phase and amplitude balance from 1 GHz to 8 GHz. The phase and amplitude differences are 2° and 0.6 dB throughout the whole band, respectively. A Monte-Carlo simulation of this active balun topology was carried out to assess the impact of variations in transistor dimensions $(W/L)_{1,2}$ and load resistors, R_1 and R_2, on the gain and phase imbalances. That simulation consisted of 1000 trials and the results show that this design is very robust with 970 trials showing a gain imbalance within a 0.4 dB window and 980 trials had a phase imbalance within a 1° window.

A schematic of the OTA circuit is shown in Fig.4 [5]. It is a low-power, very wideband circuit that uses an active inductor load and relies on a feedforward-regulated cascode topology. The feedforward approach makes it suitable for low supply voltages while retaining high linearity and high speed performance [6], [7]. A folded active inductor topology is employed here to improve the high frequency performance [8]. It is important that the transconductance of the OTAs has a linear dependence on the dc bias current to ensure that the constellation points are correctly spaced thus leading to a low EVM. In our case we used the dc voltage V_c (see Fig. 4) to control the output current. Two specific control voltages are chosen by $b_{2,3}$ to produce the basic vectors with different magnitudes. The serial resistance and total parasitic shunt capacitance at V_c set the bandwidth for the baseband signal. Furthermore, the noise contribution from OTA and the

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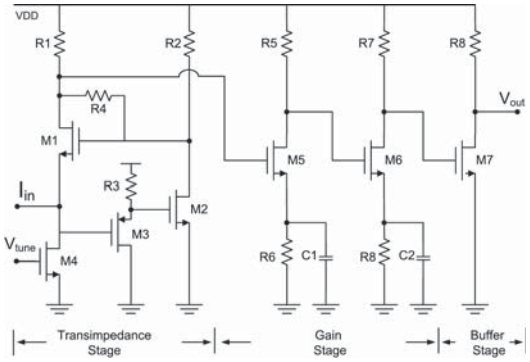

Fig. 5. Schematic of the RGC TIA

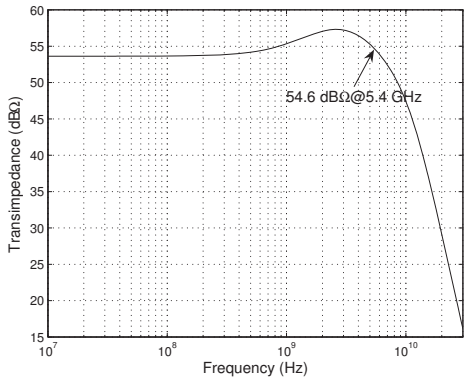

Fig. 6. Transimpedance gain of the TIA at V_{tune}= 0.75 V

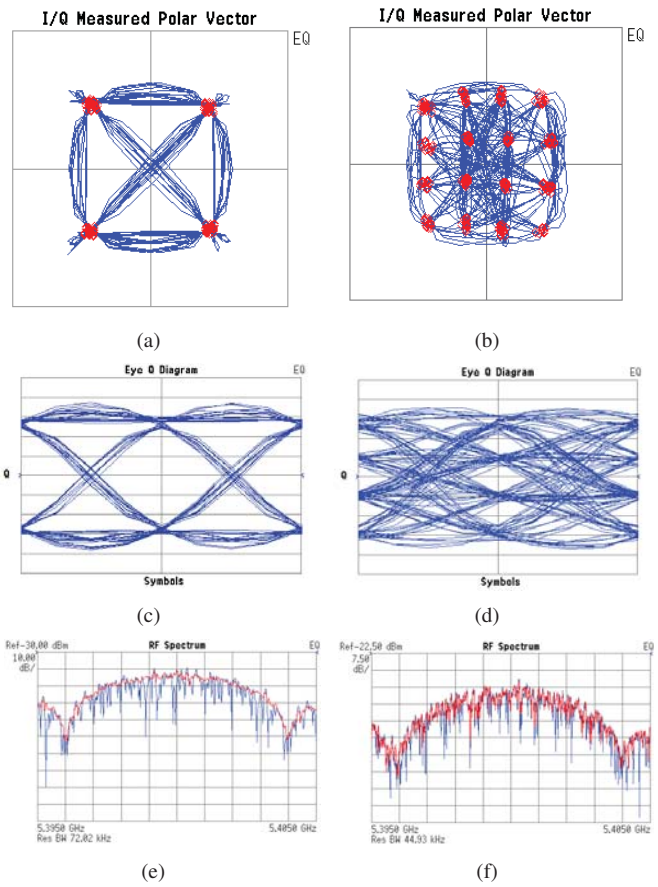

Fig. 7. Measured constellations of 4 QAM (a), 16 QAM (b), eye diagram of 4 QAM (c), 16 QAM (d) and output spectrum of 4 QAM (e),16 QAM (f)modulation at 4Msymbol/s and P_{LO}=-19 dBm.

mismatch between the I and Q OTAs will degrade the EVM performance of the modulator. To reduce the noise of the OTA and design appropriate baseband bandwidth to limit the noise from control node V_c is thus beneficial for the overall EVM performance.

The switch network shown in Fig. 1 consists of switch NMOS transistors and bypass NMOS transistors. When the switch transistor is turned off, the bypass transistor is turned on to by-pass the output current. It also provides a load impedance same as that when the switch transistor is turned on, hence this makes the OTA work in its proper region all the time.

The function of the TIA in this modulator is to provide a small load impedance for the OTAs plus a certain amount of gain. Fig. 5 shows the schematic of the TIA used in the reconfigurable modulator. It consists of a transimpedance stage, a gain stage and a common source output buffer. The input stage adopts the widely used regulated cascode (RGC) topology. By using a p-type source follower [9], [10] consisting of M3 and R3, the DC voltage at the drain of M4 can be lowered to augment the output swing at the drain of M1, which is especially suitable for low supply design. Two gain stages are added to further increase the transimpedance gain. Capacitive degeneration is used here to compensate the dominant pole with a zero, which will extend the bandwidth. Fig.6 shows the post-simulated transimpedance gain of the TIA in the frequency domain. The transimpedance at 5.4 GHz is 54.6 dBΩ and the 3 dB bandwidth is 8 GHz.

III. Measurement Results

On-wafer measurements were done using CPW probes. An off-chip 90° hybrid was used to provide the quadrature input signal to the modulator 5.4 GHz. One Agilent 81130A Pulse/Pattern Generator with two outputs and two Tektronix AFG310 Arbitrary Function Generators were employed to generate the four independent pseudo-random binary sequences (PRBS). They are synchronized via the trigger-in and trigger-out ports. An Agilent E4446A Spectrum Analyzer with digital modulation analysis option was utilized to measure the performance of the modulator. Two digital DC power supplies were used to provide the voltages for V_{DD} and V_{tune}. Due to the 10 MHz IF bandwidth limitation of the Spectrum Analyzer as well as pseudo-random binary sequence (PRBS) frequency limitation of Arbitrary Function Generators, the symbol rate was set to 4 Msymbol/s, which results a total data rate of 16 Mbit/s for the 16 QAM modulator. Yet, simulation results show that this modulator can reach data rates of up to 100 Mbit/s.

The measured constellation, eye diagram and spectrum of the modulated output signal of the chip in the 4 QAM and 16 QAM modes are shown in Fig.7. The output signal power in the 16 QAM mode was -19 dBm with an input power of -

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TABLE I
PERFORMANCE SUMMARY OF THE MODULATOR

Modulation Scheme	EVM (%)	Mag Error (%)	Phase Error degree	Freq Error (Hz)	DC offset (dB)	SNR (dB)	Output Power (dBm) $@P_{in} = -19dBm$
4-QAM	2.33	1.43	1.12	-12.59	-22.13	32.14	-27.99
16-QAM	6.20	4.40	4.05	-139.96	-26.16	21.23	-21.59

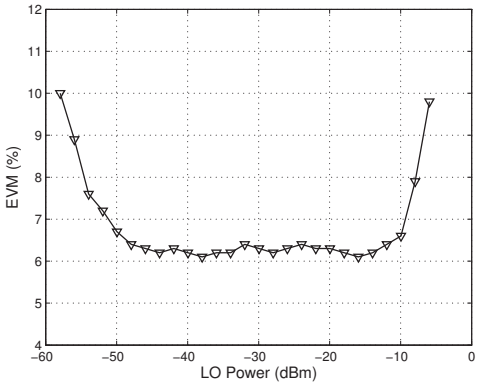

Fig. 8. Measured EVM variation of 16 QAM modulation against LO power.

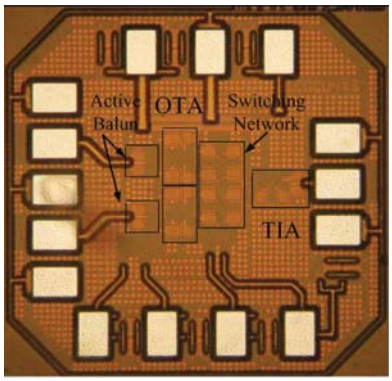

Fig. 9. Photograph of fabricated QAM modulator

21.59 dBm. The performance summary of the modulator in the 4 QAM and 16 QAM modes is listed in Table I. The EVM of the 16 QAM modulation against the input LO power is shown in Fig.(8). When the input LO power is strong, due to the gain compression and nonlinearity, the EVM degrades. Similarly, at low LO power as the sensitivity of the modulator gets close to the limitation, EVM deteriorates as well. From Fig.(8), we can see that the EVM increases by 1% in the range of input LO power from -52 to -8 dBm.

The DC power dissipation for the chip in the 16-QAM mode is 20 mA and in the 4-QAM mode is 19 mA from a 1.2 V supply voltage, including 7 mA consumed by the output buffer. The chip core measured 0.09 mm^2. A photograph of the fabricated chip is shown in Fig.9.

IV. CONCLUSIONS

A new reconfigurable QAM modulator in 0.13-μm CMOS was presented, which can be reconfigured to operate in 4, 16, or higher QAM formats. The key components of the modulator were a switch network and two high-speed OTAs with wide and linear transconductance tuning range which were used to change the magnitude of the constellation basis vectors.

V. ACKNOWLEDGMENTS

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REFERENCES

[1] A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 12, pp. 1399 –1410, Dec 1995.

[2] K. Nakajima, N. Suematsu, K. Murakami, T. Takagi, H. Nakase, Y. Isota, and K. Tsubouchi, "A 5GHz-band SiGe-MMIC quadrature modulator using a circular polyphase filter for 1Gbps transmission," vol. 2, p. 4 pp., 4-6 2005.

[3] T.-M. Chen, Y.-M. Chiu, C.-C. Wang, K.-U. Chan, Y.-H. Lin, M.-C. Huang, C.-H. Lu, W.-S. Wang, C.-S. Hu, C.-C. Lee, J.-Z. Huang, B.-I. Chang, S.-C. Yen, and Y.-Y. Lin, "A Low-Power Fullband 802.11a/b/g WLAN Transceiver With On-Chip PA," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 983–991, May 2007.

[4] H.-o. Ueda, K. Nakajima, G. Kanazawa, M. Shimozawa, J. Koide, M. Uesugi, R. Takeuchi, N. Suematsu, Y. Isota, S. Kameda, H. Nakase, T. Takagi, and K. Tsubouchi, "A 5GHz-band SiGe-MMIC transceiver for 324Mbps transmission," in *IEEE Radio and Wireless Symposium*, 2008, pp. 791–794.

[5] J. Xu, C. E. Saavedra, and G. Chen, "Wideband Microwave OTA with Tunable Transconductance Using Feedforward Regulation and an Active Inductor Load," *IEEE NEWCAS Conference*, June, 2010.

[6] Y. Zheng and C. Saavedra, "Feedforward-Regulated Cascode OTA for Gigahertz Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 11, pp. 3373–3382, Dec. 2008.

[7] Y. Zheng and C. E. Saavedra, "Full 360° Vector-Sum Phase-Shifter for Microwave System Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 4, pp. 752–758, April 2010.

[8] C.-H. Wu, J.-W. Liao, and S.-I. Liu, "A 1V 4.2mW fully integrated 2.5Gb/s CMOS limiting amplifier using folded active inductors," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 1, May 2004, pp. I–1044–7 Vol.1.

[9] C.-T. Chan and O.-C. Chen, "Inductor-less 10Gb/s CMOS transimpedance amplifier using source-follower regulated cascode and double three-order active feedback," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 0-0 2006, pp. 4 pp.–5490.

[10] Z. Lu, K. S. Yeo, J. Ma, M. A. Do, W. M. Lim, and X. Chen, "Broad-Band Design Techniques for Transimpedance Amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 3, pp. 590–600, March 2007.

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