Noise Analysis of the CG-CS Low Noise Transconductance Amplifier

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***Abstract*—In this paper, noise analysis for a low noise transconductance amplifier (LNTA) is performed. LNTA becomes popular and necessary as the high linearity requirement and low supply voltage trend make the RF front-end design go into current domain. Common-gate common-source (CG-CS) topology is examined for noise analysis. Via theoretical analysis and specific equations derived, this paper not only studies how to arrange the topology and how to choose the design parameters, but also discusses the tradeoffs existing in LNTA design between noise figure, input matching and linearity.**

I. Introduction

While CMOS technology moves into deep-submicron nodes, lower supply voltages compromise the linearity performance of circuits. One approach to address linearity requirements in RF circuits is to process signals in the current domain. The current-domain circuits have the nature of high linearity and wide operating frequency band.

Besides the issue of linearity, when the transconductance amplifier (TA) is used as the first stage of a receiver, the noise performance is also of great importance. Widely used in the wideband current-domain front-end , such as the popular front-end configuration in software defined radio (SDR) [1], [2], the low noise transconductance amplifier (LNTA) has recently drawn considerable interest. It basically employs the noise canceling topology and achieves a large transconductance value to reduce the noise factor while achieving wideband impedance matching at the input port. After examining several low noise techniques, such as common gate amplifier, resistance feedback [3] and capacitive cross coupling [4], we concentrate on common-gate common-source (CG-CS)topology.

II. noise analysis

From reviewing the CG-CS noise canceling balun-LNA [5], we know that the noise and distortion from the CG transistor will be canceled at the output port. Then its noise factor can be expressed as:

$$F = 1 + \gamma\frac{R_{CS}}{R_{CG}} + \frac{R_S}{R_{CG}}(1 + \frac{R_{CS}}{R_{CG}}) \qquad (1)$$

where R_S, R_{CS} and R_{CG} are source resistance and load resistances at the CS stage and CG stage outputs, respectively. As an example, if $\gamma = 1$ and $R_{CG} = 4R_{CS} = 4R_s$, the noise figure can be as low as 1.94 dB.

A. TA with current source

However, symmetrical infinite output impedance and low impedance load are usually assumed in the transconductance amplifiers in Fig. 1(a). Given that $R_{CG} = R_{CS}$ in (1), the noise factor is no less than $1+\gamma$. The half circuit of the differential transconductance amplifier with current source is shown in Fig 1(b). Considering the CG-CS stage as a whole (G_m), the total noise contribution of the transconductor is i_{n,G_m}. Assuming the transistors have infinite output impedance, the noise factor of TA with current source can be written as:

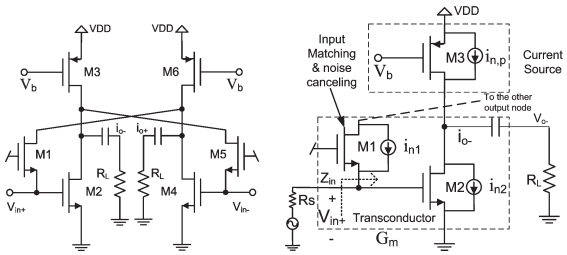

Fig. 1. The schematic of TA with current source (a) and its half-circuit small signal model for noise analysis (b).

$$F = 1 + \frac{\overline{i^2_{n,G_m}}R_L^2}{4kTR_s^{-1}A_V^2(Z_{in}//R_s)^2} + \frac{\overline{i^2_{n,p}}R_L^2}{4kTR_s^{-1}A_V^2(Z_{in}//R_s)^2} + \frac{R_L}{R_s^{-1}A_V^2(Z_{in}//R_s)^2} \qquad (2)$$

where the second term represents the noise contribution from the transconductor (M1+M2), the third term from the current source M3, and the last term from the load resistor R_L, while the voltage gain A_V equals G_mR_L. On matched condition where the input impedance has been matched to $R_S = 50\Omega$, (2) can be changed to

$$F = 1 + \gamma_n + \frac{4\gamma_p g_{mp}}{R_s G_m^2} + \frac{4}{R_S R_L G_m^2} \qquad (3)$$

where γ_n and γ_p are the noise coefficients of NMOS and PMOS, respectively. From (3), it can be inferred that the transconductance of the current source g_{mp} should be minimized and the transconductance G_m of the transconductor should be maximized to reduce the noise contribution of the current source. Also, G_m and R_L should be large to

978-1-4577-1997-4/11/$26.00 ©2011 IEEE

suppress the noise from the following stages. However, the concept of designing large G_m and R_L contradicts high linearity requirement. So linearity and NF have a tradeoff in transconductance amplifier design.

B. TA with complementary CS transconductor

From the analysis in II-A, we know that complementary common source stage should be applied to eliminate the noise contribution of the current source and increase the transconductance at the same time. Besides, in RF circuit design, the simpler the schematic is, the less noise sources are introduced and the better performance would be obtained. The schematic shown in Fig. 2(a) is spared of any redundant components.

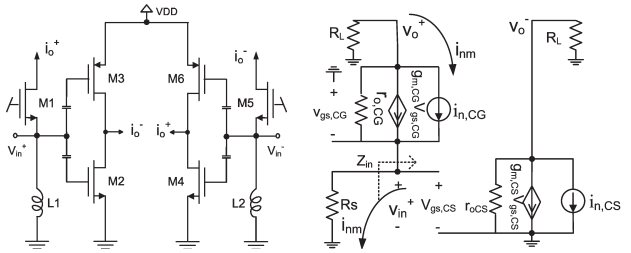

Fig. 2. The schematic of transconductance amplifier with complementary CS stage (a) and its half-circuit small signal model for noise analysis (b).

In Fig. 2(b), assuming $r_{o,CG,CS} >> R_s, R_L$ and $g_{m,CG}r_{o,CG} >> 1$, the noise current i_{nm}, the input impedance Z_{in} and the voltage gain A_v are derived as follows:

$$i_{nm} \approx \frac{i_{n,CG}}{1+g_{m,CG}R_s} \overset{R_s=Z_{in}}{\Longrightarrow} \frac{1}{2}i_{n,CG} \tag{4}$$

$$Z_{in} \approx \frac{1}{g_{m,CG}} \tag{5}$$

$$A_V \approx (g_{m,CG}+g_{m,CS})R_L = g_{m,tot}R_L \tag{6}$$

where $g_{m,CS}$ represents the total transconductance of the CS transistors, M2/M3. and the noise factor can be derived as

$$F = 1 + \frac{\gamma_n g_{m,CG}(g_{m,CS}R_s-1)^2}{R_s g_{m,tot}^2} + \frac{4(\gamma_n g_{mn,CS}+\gamma_p g_{mp,CS})}{R_s g_{m,tot}^2} + \frac{4}{R_s R_L g_{m,tot}^2} \tag{7}$$

If $g_{m,CS} = \frac{1}{R_s}$, the second term can be canceled . But now $g_{m,tot} = 40mS$ is too small to suppress the noise from the next stage. Thus, noise from M1 is usually partially canceled. Under the condition of input port matching, e.g. $g_{m,CG} = \frac{1}{R_s}$, $g_{m,tot} = g_{m,CS} + \frac{1}{R_s}$ and $\gamma_n = \gamma_p = \gamma$, we get

$$F = 1 + \gamma + \frac{4}{R_s R_L g_{m,tot}^2} \tag{8}$$

From (7) and (8), we know that the combined noise contribution of the CG and CS stages is always γ in condition of input matching for TA design. Therefore, it is important to choose a process with low noise characteristics. Considering the noise contribution of the load, it is preferred to choose a large value of the total transconductance $g_{m,tot}$.

III. Simulation Result

$0.13\mu m$ CMOS technology with $\gamma_n = 1.35$ and $\gamma_p = 1$ is employed here to verify the noise analysis above. The corresponding transistors in Fig. 1(a) and Fig. 2(a) have the same feature sizes. The DC current consumption is set at 10 mA and the input matching $S11$ is limited below -10 dB up to 6 GHz in both cases. The simulation results from Fig. 1(a) and Fig. 2(a) and the calculation results from Eqn(3)and Eqn(7) are shown in Fig. 3. Although only the channel thermal noise is considered, the theoretical analysis predicts the noise figure well.

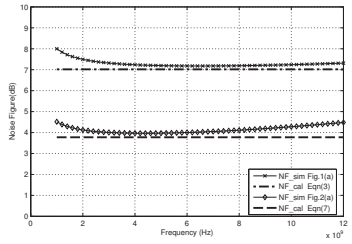

Fig. 3. The simulation and theoretical analysis results.

IV. Conclusion and Discussion

In this paper, noise analysis of a CG-CS LNTA has been performed. Wideband input impedance matching, low noise and high linearity are usually required for LNTA. To eliminate the noise contribution of the current source, the complementary inverter CS stage should be employed. In case of input matching, the CG-CS transistors will always contribute a factor of γ in the noise factor expression no matter how to choose $g_{m,CG}$ and $g_{m,CS}$. So choosing the technology with small γ is important for LNTA design. For the sake of low noise requirement, the total transconductance $g_{m,tot}$ is preferred to be large to suppress the noise contribution of the following stage. However, the large total transconductance brings on higher voltage gain which deteriorates linearity performance. So low noise, input matching and linearity should be carefully traded off in LNTA design.

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