A CMOS Amplifier with Third-Order Intermodulation Distortion Cancellation

Brad R. Jackson and Carlos E. Saavedra
Department of Electrical and Computer Engineering
Queen's University
Kingston, Ontario, Canada, K7L 3N6
Email: carlos.saavedra@queensu.ca

***Abstract*—A 2.4 GHz CMOS amplifier with third-order intermodulation distortion cancellation is presented based on the derivative superposition technique. The proposed circuit uses a conventional amplifier topology followed by a distortion cancellation circuit that can significantly improve third-order linearity. To quantify the linearity improvement, two general-purpose amplifiers were fabricated and measured: (1) a traditional cascode amplifier and (2) an identical cascode amplifier followed by a distortion cancellation circuit. The new amplifier increases the IP_3 by approximately 12 dB without having a significant effect on either the gain or noise characteristics of the original amplifier.**

I. Introduction

The intermodulation distortion (IMD) of an amplifier, in addition to gain, noise figure, and 1-dB compression point, is a very important consideration in many applications. To characterize the IMD of an amplifier, the most common method used is the third-order intermodulation product intercept point (IP_3). This method is based on the common situation where the desired signal is in the presence of an interferer that is nearby in the frequency domain. The third-order nonlinearities of an amplifier generate new tones that are close to the desired tone that can cause interference.

There have been several methods suggested that can potentially improve the linearity of CMOS amplifiers. These include: predistortion, feedback, feedforward, optimal biasing, and derivative superposition.

Predistortion techniques rely on the ability to distort the input signal to an amplifier such that it is the inverse of the amplifier nonlinearity and is most commonly used in power amplifiers (e.g. [1]). In [2], active feedback was used to linearize a low-noise amplifier (LNA), but in some cases the noise figure can be seriously degraded using this technique. Feedforward distortion cancellation was used in both [3] and [4]. While a high IP_3 was obtained in [3], only simulation results are shown. In [4], a duplication of the original amplifier is required, which doubles the power consumption, and also requires different input signal power levels for the main and auxiliary amplifier circuits. The optimal biasing technique relies on the accurate biasing of the transistors such that the third-order nonlinearity coefficient is zero. While this technique has been demonstrated with good results (e.g. a 10.5 dB IP_3 improvement in [5]), it is very sensitive to bias variations. The derivative superposition technique uses parallel transistors with different biases such that when the signals are summed, the distortion terms are cancelled. Two or more FETs are used in parallel with different bias points and widths in order to control the distortion at the output. This technique has been used in [6]–[8] with measured IP_3 improvements of 10 dB or more. A typical derivative superposition circuit is shown in Fig. 1 with two FETs. This circuit is most commonly used used to control the third-order intermodulation (IM3) distortion by separately biasing the two FETs in Fig. 1 such that one has a positive third-order coefficient and the other a negative third-order coefficient with equal magnitudes. This can result in a significant improvement in the IP_3 of an amplifier. In [6], derivative superposition was used in a cascode amplifier design by adding an additional common-source transistor in parallel with the original common-source transistor (each with appropriate gate bias and device width).

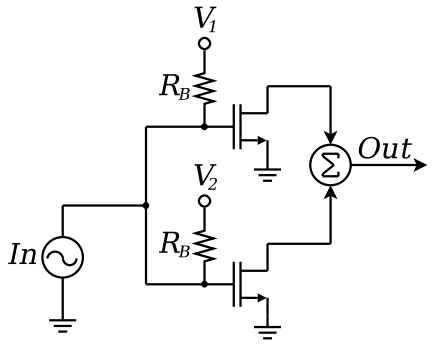

Fig. 1. Derivative superposition with two FETs.

In this work, the derivative superposition technique is used *after* the amplifier to cancel the third-order intermodulation products generated by the amplifier. Whereas the previously mentioned techniques are generally integrated into the initial amplifier design, this topology opens the possibility of enhancing the linearity of a pre-existing amplifier by following it with a distortion cancellation circuit. Furthermore, since the distortion cancellation circuit is connected to the output of the amplifier, its effect on the noise figure can be greatly reduced. Measurement results of the proposed technique show a very minor effect on the gain and noise figure characteristics of the original amplifier, but a significant improvement in the IP_3.

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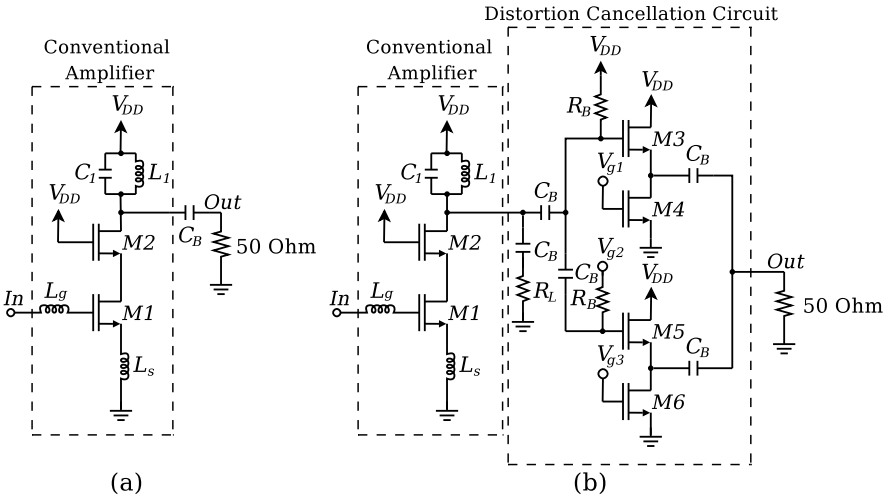

Fig. 2. (a) Conventional cascode amplifier and (b) cascode amplifier with third-order IMD cancellation.

II. Distortion Cancellation Technique

The circuit diagram for a conventional general-purpose cascode amplifier is shown in Fig. 2(a). This very common amplifier uses inductors L_g and L_s for matching and the parallel tank circuit, C_1 and L_1, in addition to any parasitic capacitance, is designed to resonate at the desired frequency. Shown in Fig. 2(b) is the amplifier with third-order IMD cancellation, which consists of the original amplifier shown in Fig. 2(a), followed by a distortion cancellation circuit.

In general, the output drain current of a FET amplifier can be described by the power series:

$$i_d = g_{m1}v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3 + ... \tag{1}$$

where

$$g_{mn} = \frac{\partial^n I_D}{\partial V_{GS}^n} \tag{2}$$

are the coefficients of the fundamental ($n = 1$) and higher-order ($n > 1$) terms that lead to nonlinearities. The IP_3 performance is predominantly determined by the third-order nonlinearity coefficient, g_{m3}. The IIP_3 for an amplifier with a 50 Ω input impedance is given by [9]:

$$IIP_3 = 10\log\left(\frac{40}{3}\left|\frac{g_{m1}}{g_{m3}}\right|\right) \quad \text{dBm} \tag{3}$$

It is well known that the g_{m3} coefficient can be either positive or negative, depending on the biasing conditions (e.g. see [5]). In fact, g_{m3}, changes from positive to negative as the FET transitions from the weak to strong inversion regions, as shown in Fig. 3. The ability to control the sign of the third-order coefficient is the property used in this work to design a amplifier with third-order IMD cancellation.

The distortion cancellation circuit is simply two parallel source-follower buffers. The load resistor, R_L, is designed to be somewhat greater than 50 Ω so that the resulting increased voltage amplitude is equal to the loss through the buffer consisting of transistors *M3* and *M4*. The result is a fundamental output that is very similar to the original amplifier in Fig. 2(a). The auxiliary path through the buffer *M5* and *M6* is designed with appropriate biasing and device sizes such that the third-order nonlinearity current that is generated is equal in magnitude to the the primary path, but 180° out of phase. The phase inversion is achieved by biasing *M3* and *M5* independently in the negative and positive g_{m3} regions, respectively. For the primary path, through *M3* and *M4*, the required V_{GS} will typically be in the strong inversion region, and thus will have a negative g_{m3}. The auxiliary path through *M5* and *M6* is therefore biased through V_{g2} and V_{g3} to be in the weak inversion region where there is a positive g_{m3}. The resulting third-order nonlinearity currents are summed at the output, resulting in distortion cancellation. Since the fundamental signal maintains the same sign for both buffer circuits, it is added in-phase, thus increasing the fundamental output power. However, since a positive g_{m3} occurs in the weak or moderate inversion regions, the contribution of the auxiliary path to the fundamental output power is much

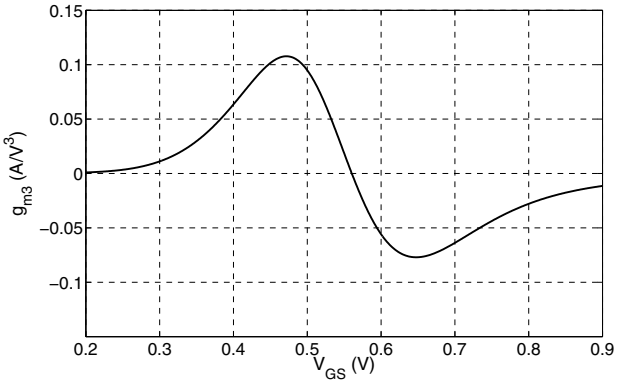

Fig. 3. Typical third-order nonlinearity coefficient, g_{m3}.

smaller than from the primary path (since g_{m1} is small in the weak and moderate inversion regions).

Consider two input signals to the amplifier shown in Fig. 2(b) with different frequencies, f_1 and f_2. The output of the "Conventional Amplifier" includes the fundamental signals, f_1 and f_2, as well as the IM3 signals generated in the cascode amplifier ($2f_1 \pm f_2$ and $2f_2 \pm f_1$). The IM3 products at the output of *M3–M4* include the contribution of the IM3 signals generated by the cascode amplifier that were inputs to the distortion cancellation circuit, as well as the IM3 signals generated in *M3–M4* from the amplified f_1 and f_2 signals. The *M3–M4* buffer is biased such that the g_{m3} coefficient is negative. The auxiliary path *M5–M6* buffer is designed to be in the positive g_{m3} region, and it therefore produces IM3 products that are opposite in phase relative to those generated by the *M3–M4* buffer. By designing each source-follower buffer in the distortion cancellation circuit to generate overall IM3 currents that are equal in magnitude, but 180° out of phase, it is possible to significantly improve the IP3 of the amplifier by summing these currents at the output.

In order to choose the bias points that result in optimal distortion cancellation, existing BSIM3 FET models were used in simulations for this work and they resulted in very accurate predictions. If accurate device models are not available, this technique can still be used, but IM3 measurements for the chosen technology may be necessary to achieve optimal performance.

III. Measurement Results

The supply voltage for both amplifiers was set to 1.8 V and the bias voltages on the third-order IMD cancellation amplifier were $V_{g1} = 1.0$ V, $V_{g2} = 0.52$ V, and $V_{g3} = 1.5$ V. To characterize the performance of both of the amplifiers, a full two-port calibration was performed and the S-Parameters were measured using a vector network analyzer. The results are shown in Fig. 4. It is clear that both amplifiers have very similar S_{11} and S_{21} characteristics. Note that the amplifier with third-order IMD cancellation achieves a slightly higher gain and a slightly larger bandwidth. For both amplifiers the gain and return loss at 2.4 GHz are approximately 16 dB and -10 dB, respectively.

To determine the linearity of each amplifier, a two-tone input signal (2.400 GHz and 2.401 GHz) was used and the output power of the third-order distortion was measured. Shown in Fig. 5 is the output spectrum for both amplifiers superimposed so that the difference in third-order intermodulation distortion is clear. The input power used for each tone was -30 dBm. It is not possible to distinguish between the two amplifiers with regards to the fundamental outputs. For both amplifiers, the two fundamental outputs show a power of approximately -14 dBm as expected since the measured S_{21} was approximately 16 dB. The third-order intermodulation distortion products occur at 2.399 GHz and 2.402 GHz ($2f_1 - f_2$ and $2f_2 - f_1$) for this two-tone test. In the case of the conventional amplifier, the output power of the third-order intermodulation products is approximately -67 dBm (dashed line). In the case of the amplifier with distortion cancellation, the third-order intermodulation products have been significantly attenuated by approximately 21 dB (solid line). These two plots clearly illustrate that the proposed distortion cancellation method can provide much improved third-order linearity performance. The IP_2 performance of the amplifier is degraded somewhat with this technique, however, since the second-order distortion signals are far out of band (1 MHz and 4.801 GHz in this case) this is not a major concern in most systems.

The input power of the two input tones were then swept for each amplifier while the fundamental and third-order distortion output powers were measured. The results are shown in Fig. 6. The IIP_3 of the conventional amplifier is approximately -2 dBm whereas the IIP_3 of the amplifier with distortion

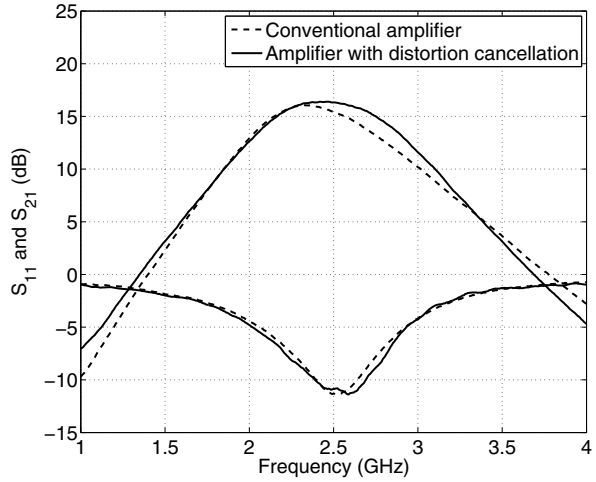

Fig. 4. Measured S_{21} and S_{11} of the conventional and distortion cancellation amplifiers.

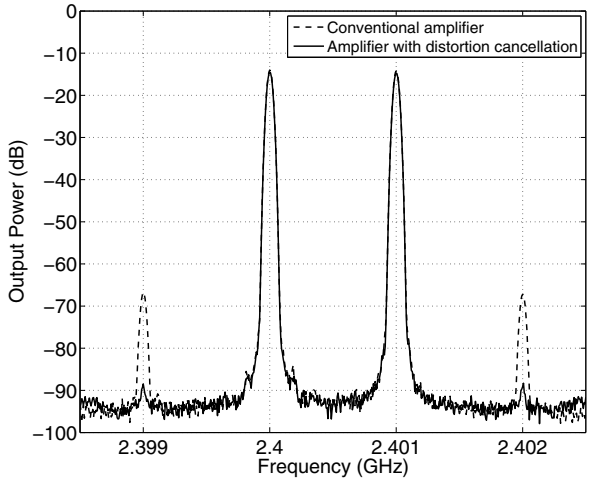

Fig. 5. Superimposed spectra of both amplifiers with two input tones at 2.400 GHz and 2.401 GHz (-30 dBm input power).

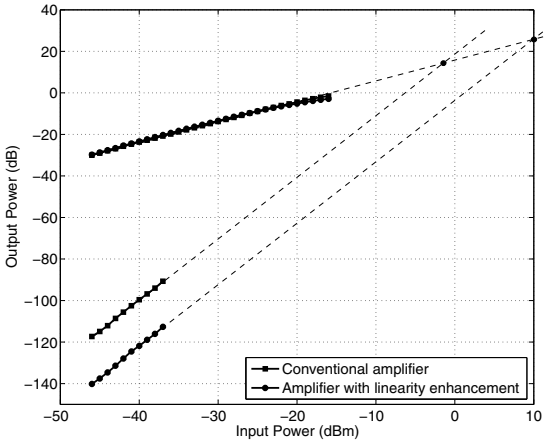

Fig. 6. IP_3 measurements for the original and distortion cancellation amplifiers.

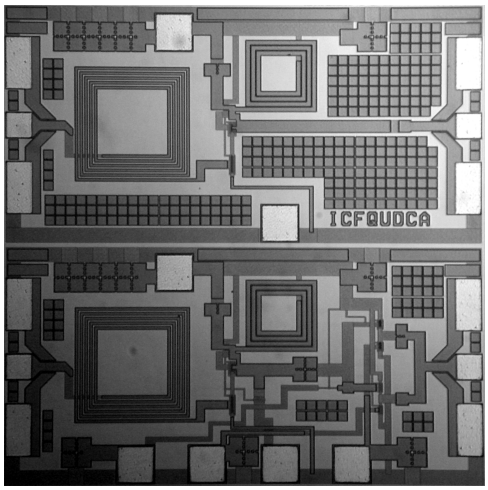

Fig. 7. Microphotograph of the fabricated amplifier circuits (top is the conventional amplifier and bottom is the new amplifier with IP_3 enhancement.

cancellation is approximately 10 dBm. Therefore, a +12 dB improvement in IIP_3 was measured using the proposed technique. With the distortion cancellation amplifier, the 1-dB compression point is reduced by approximately 3 dB, however, this may not be a significant concern in many cases where there is a low input power level (e.g. in a low-noise amplifier).

The noise figure of each amplifier was measured to determine the effect of the distortion cancellation circuit on the noise performance. At 2.4 GHz, the noise figure of the conventional amplifier is 4.02 dB, while the noise figure of the third-order IMD cancellation amplifier is 4.18 dB, an increase of just 0.16 dB. Therefore, there is not a significant degradation in the noise figure with this technique.

The DC current used by the conventional amplifier was 21 mA and for the distortion cancellation amplifier it was 31 mA. The added current in the proposed amplifier is due almost entirely to the *M3–M4* source-follower circuit shown in Fig. 2(b). A commonly used figure of merit for for low-noise amplifiers is defined as [10]:

$$FOM = \frac{OIP_3}{(F-1)P_{DC}} \tag{4}$$

where OIP_3 is the output-referred IP_3 point, F is the noise factor, and P_{DC} is the DC power consumption. The proposed amplifier achieves a FOM of 308, which compares favourably to most LNAs in the literature. A photograph of the fabricated chip is shown in Fig. 7. The dimensions of the entire chip are 1 mm $\times$ 1 mm with each amplifier using half of this space (0.5 mm^2). The additional chip area required by the proposed technique is approximately 300 μm $\times$ 200 μm (0.06 mm^2).

IV. Conclusion

A new amplifier has been described that includes a distortion cancellation circuit to significantly improve third-order linearity. The derivative superposition technique is used *after* the amplifier to attenuate third-order intermodulation products without significantly increasing the noise figure. To evaluate the effectiveness of this technique, two general-purpose amplifiers were designed – one with the distortion cancellation circuit and the other without. The result was a +12 dB improvement in the IIP_3 point with no significant affect on the gain or noise characteristics of the amplifier. This technique could be very attractive in the situation where an existing amplifier does not meet the IP_3 requirements. Rather than completely redesign the amplifier for improved linearity performance, the proposed technique could be used to improve the intermodulation distortion by following the existing amplifier with a distortion cancellation circuit.

References

[1] G. Hau, T. B. Nishimura, and N. Iwata, "A highly efficient linearized wide-band CDMA handset power amplifier based on predistortion under various bias conditions," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 49, pp. 1194–1201, June 2001.

[2] K. W. Kobayashi, D. C. Streit, A. K. Oki, D. K. Umemoto, and T. R. Block, "A novel monolithic linearized HEMT LNA using HBT tunable active feedback," *IEEE MTT-S International Microwave Symposium Digest*, Vol. 3, pp. 1217–1220, June 1996.

[3] M. Lin, Y. Li, and H. Chen, "A novel IP_3 boosting technique using feedforward distortion cancellation method for 5 GHz CMOS LNA," *IEEE Radio Freq. Integrated Circuits Symp.*, pp. 699–702, June 2003.

[4] Y. Ding and R. Harjani, "A +18 dBm IIP_3 LNA in 0.35 μm CMOS," *IEEE International Solid-State Circuits Conference*, pp. 162–164, 2001.

[5] V. Aparin, G. Brown, and L. E. Larson, "Linearization of CMOS LNA's via optimum gate biasing," *IEEE International Symposium on Circuits and Systems*, Vol. 4, pp. 748–751, May 2004.

[6] V. Aparin and L. E. Larson, "Modified derivative superposition method for linearizing FET low-noise amplifiers," *IEEE Trans. on Microwave Theory and Techniques*, Vol. 53, No. 2, pp. 571–581, February 2005.

[7] D. Webster, J. Scott, and D. Haigh, "Control of circuit distortion by derivative superposition method," *IEEE Microwave and Guided Wave Letters*, Vol. 6, No. 3, pp. 123–125, March 1996.

[8] D. R. Webster, et. al., "Low-distortion MMIC power amplifier using a new form of derivative superposition, " *IEEE Trans. on Microwave Theory and Techniques*, Vol. 49, No. 2, pp. 328–332, Feb. 2001.

[9] T. T. Ha, *Solid-State Microwave Amplifier Design*, New York: Wiley, ch. 6, 1981.

[10] D. C. Ahlgren, N. King, G. Freeman, R. Groves, and S. Subbanna, "SiGe BiCMOS technology for RF devices and design applications, " *Proc. IEEE Radio Wireless Conf.*, pp. 281–284, 1999.