Frequency Doubler Employing Active Fundamental Cancellation in CMOS

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***Abstract*—A novel CMOS frequency doubler circuit is presented in this paper. A common source transistor pair biased at threshold is used to rectify the input signal in both the positive and negative cycles. The rectified signals are then subtracted to generate a double frequency signal. Measurement results show that there is more than 20 dB fundamental rejection with the input power level ranging from -20 dBm to -10.3 dBm. The 3^{rd} and 4^{th} harmonic rejections are above 20 dB with input power up to -10 dBm without any on-chip or off-chip filtering.**

I. Introduction

Frequency multipliers have been frequently used in communication systems. With the use of the multipliers, higher frequency signal can be generated without compromising its phase noise performance because oscillators can be designed at much lower frequencies, at which the phase noise is lower. The frequency multipliers can also be used to alleviate the problem of VCO pulling.

Many frequency doubler circuits have been proposed. One that has been widely used is a single transistor biased at pinch-off with an output filter to remove the fundamental as well as to provide output matching to the 2^{nd} harmonic [1]–[3]. For low cost applications and compact devices, having large on-chip inductors is undesirable. A broadband CMOS frequency doubler that makes use of microwave baluns was demonstrated in [4] that works beyond 25 GHz. However at low frequencies, transmission lines and other microwave structures are too big to be realized on chip. Another common technique is to use two source-and-drain-coupled transistors as demonstrated in [5]. [6] expanded on this topology by cross coupling two unbalanced source-coupled pairs to double the input frequency and achieve harmonic suppression. These two approaches require a differential input feeding into the gates of the transistors while the output is taken single-endedly at the drain. However, in many applications a differential LO is more preferable. In [7], a doubler was demonstrated with good fundamental rejection at the output without using on-chip filtering. In that chip, a time-delay technique was used to generate the double frequency and to reject the fundamental.

In this paper, a novel frequency doubler design is proposed that makes use of the complementary NMOS and PMOS transistors in 0.18 μm CMOS. The doubler takes a single-ended input and produces a differential output. Two rectifiers are used to remove the lower or the upper part of the sinusoidal wave respectively. The rectified signals are then subtracted to generate the doubled frequency output. No on-chip or off-chip filtering is required with this implementation.

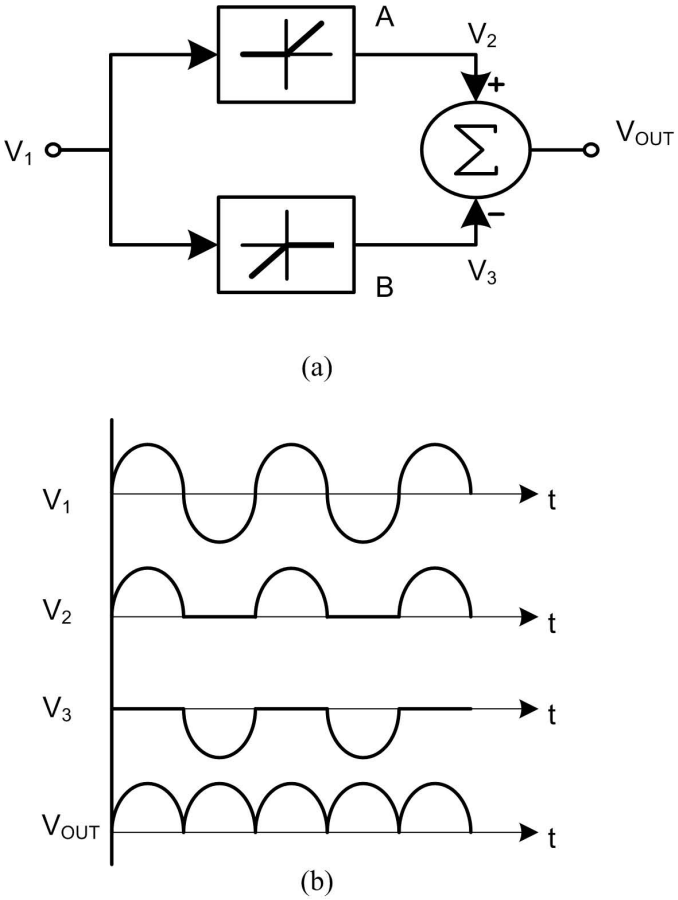

Fig. 1. (a) Frequency doubler block diagram and (b) Voltage waveforms at the associated nodes.

II. Circuit Implementation

The block diagram of the doubler is shown in Fig. 1 where blocks A and B are half-wave rectifiers. The sinusoidal source waveform at V_1 branches off into the two rectifiers, and rectifier A retains only the upper portion of the source waveform and rectifier B retains the lower portion. Their outputs are then fed into a subtractor. Since the output is a rectified version of the input, the output frequency is therefore doubled. One of the advantages of this approach is that a strong 2^{nd} harmonic signal is generated while the fundamental signal is cancelled at the same time, without the use of any filters.

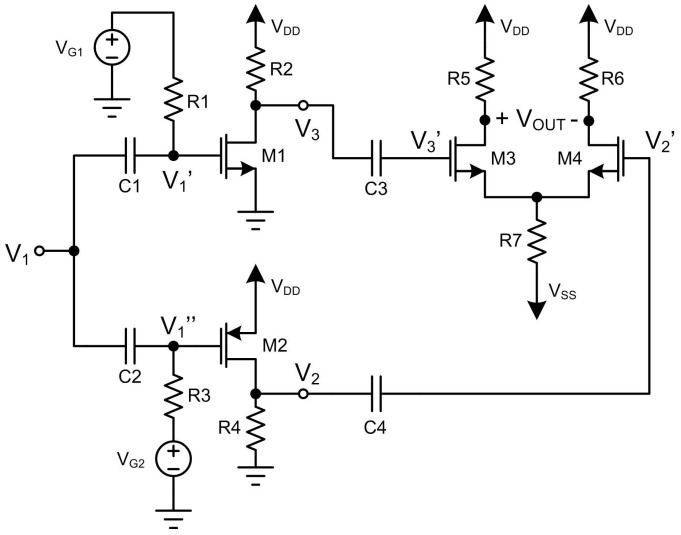

Fig. 2. Circuit diagram of the frequency doubler core.

Another advantage is that no baluns are necessary since the rectifiers are complementary. This results in a very compact and simplified circuit.

Fig. 2 shows the circuit schematic of the doubler core. The rectifier pairs are realized by the complementary NMOS and PMOS common source pairs. The gates of both common source amplifiers are biased at their respective threshold voltages, so that they only turn on during half of the cycle to produce the rectified waveforms at nodes V_2 and V_3, similar to the ones in Fig. 1. The common source configuration is used because it reduces the conversion loss of the circuit. Finally, a differential amplifier subtracts the waveforms from the drains of M1 and M2 to cancel the fundamental and generate the second harmonic.

There are two important design criteria that must be met to ensure proper fundamental cancellation. First, the gain of the rectifier pair must be the same such that there is no amplitude variation in the output signal. Second, to ensure high cancellation, the phase difference between the waveforms at nodes V_2' and V_3' must be zero. Assuming the C_{gd}'s of the transistors have negligible impact on the phase difference at the frequency of interest, the phase delay from V_1 to V_3' and from V_1 to V_2' should be equal and they are given by

$$\theta_1 = \pi + \frac{\pi}{2} - tan^{-1}[\omega R_1(C_1 + C_{gs1})] - tan^{-1}(\omega R_2 C_{gs3}) \quad (1)$$

$$\theta_2 = \pi + \frac{\pi}{2} - tan^{-1}[\omega R_3(C_2 + C_{gs2})] - tan^{-1}(\omega R_4 C_{gs4}) \quad (2)$$

where θ_1 is the phase delay from V_1 to V_3' and θ_2 is the phase delay from V_1 to V_2'.

The output can be taken directly from the output of the differential amplifier, or the differential output can be turned into a single-ended output with the use of a combiner. The latter approach was used in this work for measurement purposes. This frequency doubling technique is a very compact scheme such that the core itself only requires a total of four transistors.

An on-chip active matching network is used to achieve input impedance matching. Fig. 3 shows the complete circuit. The chip was fabricated with TSMC CMOS 0.18 μm process. The area for the core is approximately 130 μm x 140 μm (0.018mm^2) and the overall chip is 402 μm x 707 μm (0.284mm^2) including pads.

III. Simulation and Measurement Results

The circuit simulation was done in Agilent's Advanced Design System and the layout was completed in Cadence.

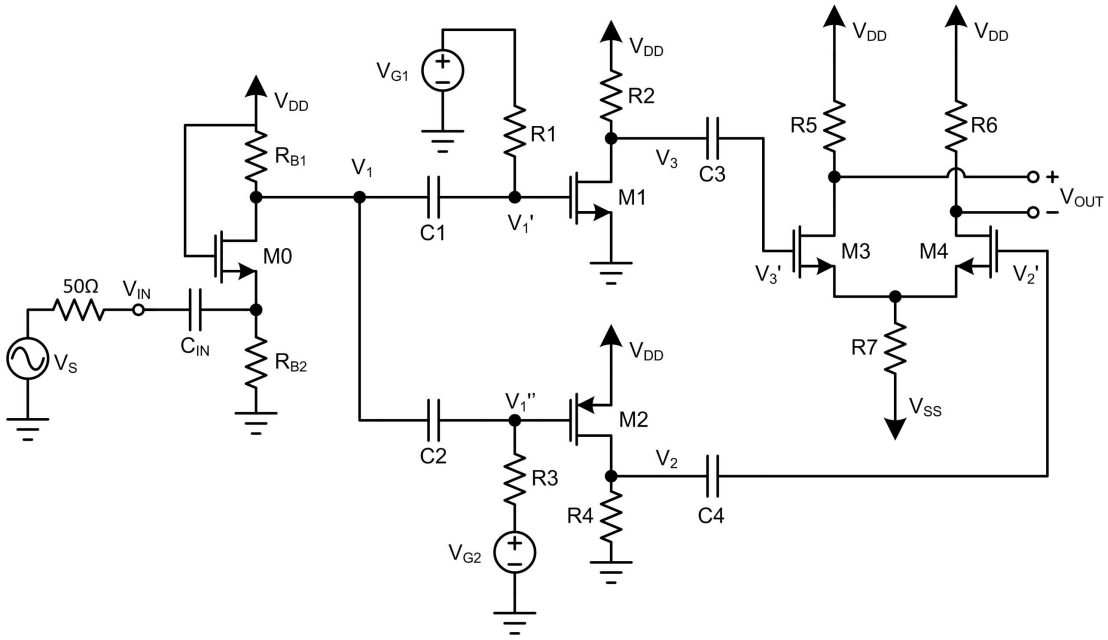

Fig. 3. The complete circuit of the frequency doubler.

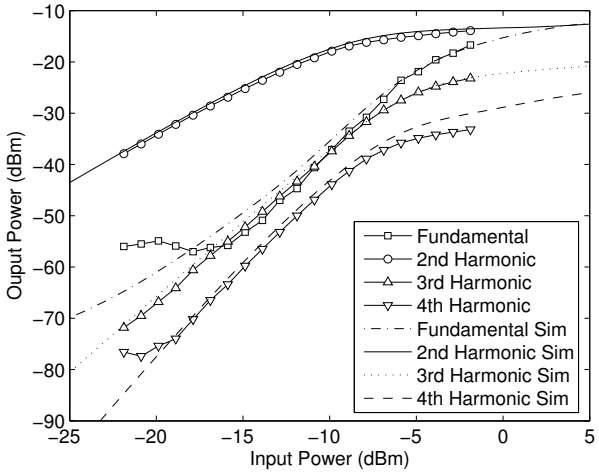

Fig. 4. Measured output powers of the harmonics with a 2 GHz input.

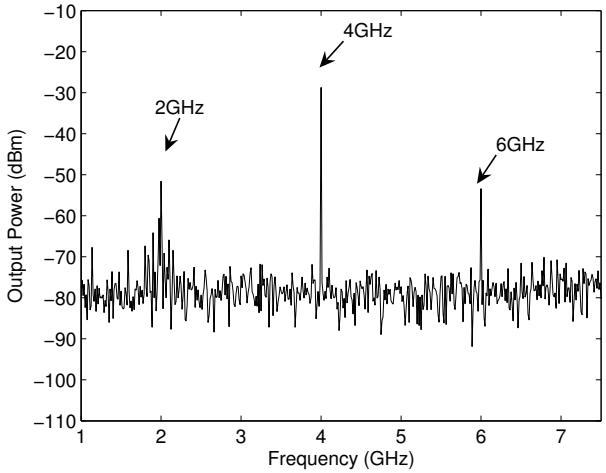

Fig. 6. Output spectrum plot with -15dbm input at 2 GHz.

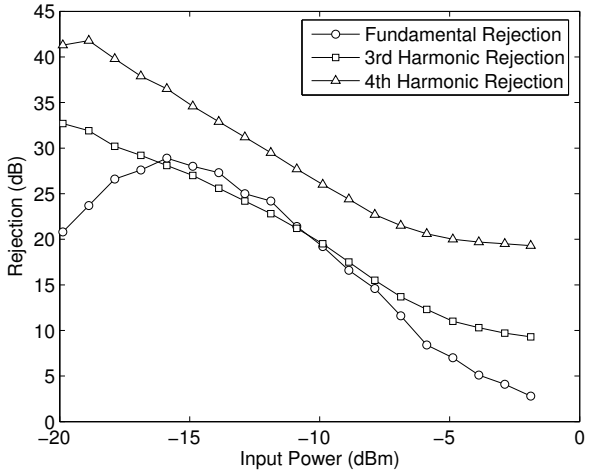

Fig. 5. Fundamental and harmonic rejections from measurements.

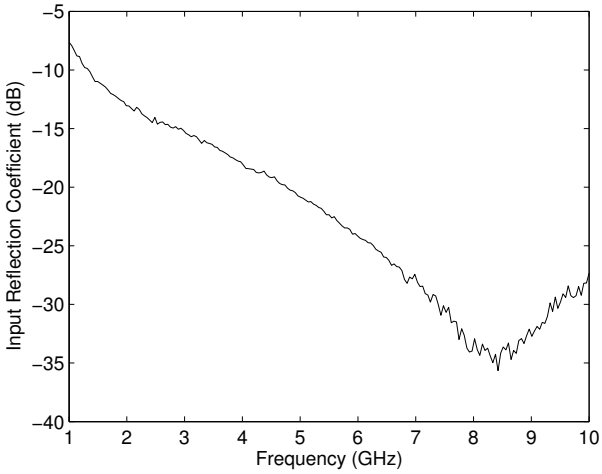

Fig. 7. Measured input reflection coefficient.

The post-layout simulation was done using the Cadence-ADS Dynamic Link.

To determine the performance of the frequency doubler, a proof-of-concept 2 GHz to 4 GHz integrated circuit was fabricated in 0.18μm CMOS. The input power level was swept and the output powers of the first four harmonics were measured using a Spectrum Analyzer. The measurement was done on wafer with the use of two CPW RF probes. Fig. 4 shows the measured and simulated output powers of the first four harmonics versus input power. The output power of the 2^{nd} harmonic at 4 GHz is the strongest, as desired. The output powers of the 3^{rd} and 4^{th} harmonic are also shown, which are substantially below the 2^{nd} harmonic.

Shown in Fig. 5 are the rejection of the fundamental, 3^{rd}, and 4^{th} harmonic with respect to the 2^{nd} harmonic. There is more than 20 dB fundamental rejection where the input power levels are between -20 dBm to -10.3 dBm. The output power levels of the 3^{rd} harmonic are at least 20 dB lower than that of the 2^{nd} harmonic with input power levels up to -10 dBm. The 4^{th} harmonic rejection is more than 20 dB with input power level up to -5 dBm. There is excellent agreement between the measured and simulated results for the fundamental, 3^{rd}, and 4^{th} harmonics. Due to the circuit sensitivity to the phase as explained earlier, parasitic resistance can affect the phase difference between V_2' and V_3', and thereby adversely affect the fundamental rejection.

The frequency doubler performs best with an input power of -15 dBm. At this power level, there is more than 25 dB rejection for the harmonics and the fundamental. Fig. 6 is the spectrum plot taken from 1 GHz to 7.5 GHz at this input power level, which further confirms the performance of the doubler. The conversion loss at this input power level is approximately 10.4 dB. Note that the CMOS common source pair is never truly off due to subthreshold current, and therefore this lowers the 2nd harmonic voltage during the subtraction, thus affecting the conversion loss.

The input reflection coefficient of the frequency doubler was measured using a Vector Network Analyzer. As shown

TABLE I
COMPARISON OF SEVERAL FREQUENCY DOUBLERS WITH THIS WORK

Reference	Technology	f_{out} (GHz)	Die Size (mm^2)	S_{11} (dB)	Fundamental Rejection (dB)	3^{rd} Harmonic Rejection (dB)	4^{th} Harmonic Rejection (dB)	Filter
[2]	CMOS 0.18 μm	5.2	0.36	-8	> 20	> 22	> 28	Yes
[7]	CMOS 0.18 μm	1.2	0.015	-	> 25	> 25	> 10	No
[3]	CMOS 0.13 μm	54.2	0.924	-	49.2	-	-	Yes
This Work	CMOS 0.18 μm	4	0.018	-13.05	> 25	> 25	> 33	No

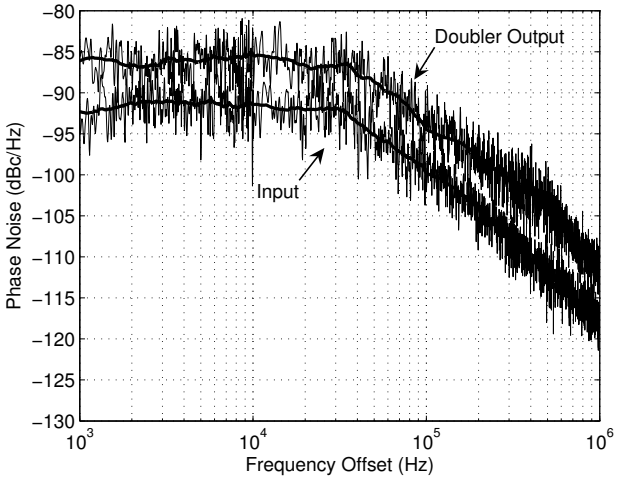

Fig. 8. Measured phase noise of the source and the frequency doubler with a 2 GHz input.

in Fig. 7, the input is reasonably matched at the frequency of interest. The input reflection coefficient at 2 GHz is -13.05 dB. The phase noise degradation of a signal passing through a multiplier is $20log(n)$, where n is the multiplication factor. For $n = 2$, the theoretical degradation is 6.02 dB. The output phase noise of the frequency doubler was measured with the same input power at -15 dBm. Fig. 8 shows the measured phase noise of the source and the doubler. The output phase noise is -111.7 dBc at a 1 MHz offset and the phase noise degradation is 6.5 dB. The DC voltages (V_{DD} and V_{SS}) supplied to the circuit are 1.8 V and -1.8 V respectively. The power consumption of the frequency doubler is 26.9 mW. Fig. 9 shows a microphotograph of the chip and Table I shows a comparison between this work and recent integrated circuit frequency doublers in CMOS.

IV. CONCLUSION

In this paper, a novel frequency doubler has been presented that achieves high output fundamental and harmonic rejection without any filtering. Using TSMC CMOS 0.18 μm technology, the circuit converts a 2 GHz input into a 4 GHz output. Measurement results show that there is more than 20 dB fundamental, 3^{rd}, and 4^{th} harmonic rejection with the input ranging from -20 dBm to -10.3 dBm. The doubler also converts a single-ended input into a differential output. The

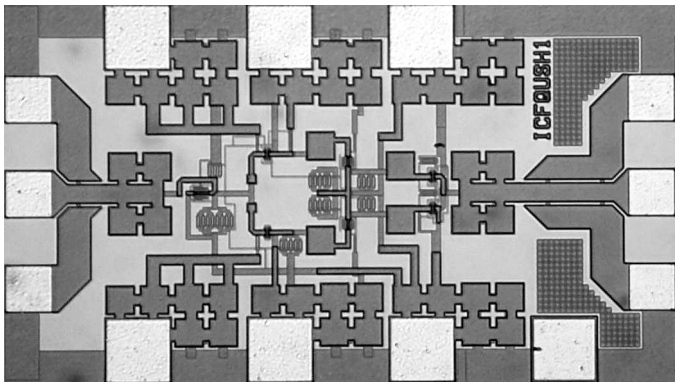

Fig. 9. Microphotograph of the complete chip.

power consumption of the circuit is 26.9 mW and the circuit core occupies an area of 0.018 mm^2.

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REFERENCES

[1] F. Ellinger and H. Jackel, "Ultracompact SOI CMOS frequency doubler for low power applications at 26.5-28.5 GHz," *IEEE Microwave and Wireless Components Letters*, vol. 14, no. 2, pp. 53–55, Feb. 2004.

[2] K. Yamamoto, "A 1.8-V operation 5-GHz-band CMOS frequency doubler using current-reuse circuit design technique," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 6, pp. 1288–1295, June 2005.

[3] D. Y. Jung and C. S. Park, "A Low-Power, High-Suppression V-band Frequency Doubler in 0.13 μm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 8, pp. 551–553, Aug. 2008.

[4] T. Y. Yang and H. K. Chiou, "A 25-75 GHz Miniature Double Balanced Frequency Doubler in 0.18 μm CMOS Technology," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 4, pp. 275–277, April 2008.

[5] K. Nimmagadda and G. Rebeiz, "A 1.9 GHz double-balanced subharmonic mixer for direct conversion receivers," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 253–256, May 2001.

[6] R. Murji and M. Deen, "A low-power wideband frequency doubler in 0.18 μm CMOS," *IEEE International Symposium on Circuits and Systems*, pp. 4353–4356 Vol. 5, May 2005.

[7] B. Jackson and C. Saavedra, "An L-band CMOS frequency doubler using a time-delay technique," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 131–134, Jan. 2006.