Coherent BPSK Demodulator MMIC Using an Anti-Parallel Synchronization Loop

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***Abstract* — A coherent BPSK demodulator using an anti-parallel synchronization loop is successfully implemented in a 0.18 μm CMOS monolithic-microwave-integrated-circuit (MMIC). Due to the novel concept of the anti-parallel synchronization method, the demodulator only requires a differential VCO as opposed to a quadrature VCO as in the Costas Loop, thereby saving considerable chip space. The fabricated demodulator works at a carrier frequency of 2.7GHz and has been tested at data rates of up to 7Mbps. The circuit measures 1.0 mm^2 including the bonding pads and consumes 151 mW of power.**

***Index Terms* — Demodulation, MMICs, phase locked loops, phase shift keying, synchronization.**

I. Introduction

Phase-shift keying (PSK) modulation is used in many wireless communication systems. Binary phase-shift keying (BPSK), for example, has been adopted in RF networks using IEEE802.11a and IEEE802.11b [1], and satellite systems such as the International Maritime Satellite (INMARSAT) System [2] and the Global Positioning System (GPS)[3]. The BPSK scheme is also used in Radio Frequency Identification (RFID) systems [4].

This paper presents a coherent BPSK demodulator using a novel anti-parallel synchronization loop, which is successfully integrated in a monolithic-microwave-integrated-circuit (MMIC) using CMOS technology. Compared to the other coherent BPSK demodulator techniques using the squaring loop [5], the re-modulator loop [6], and the Costas loop [7], the proposed demodulator is quite different in its approach. With respect to the Costas Loop, one important feature of this new demodulator is that it does not require a physically large quadrature VCO, instead it only needs a differential VCO. This results in a compact demodulator MMIC. The rest of this paper is organized as follows. The coherent BPSK MMIC with its implementation details is described in Section II and the demonstration from its measurement is presented in Section III. Section V concludes this paper.

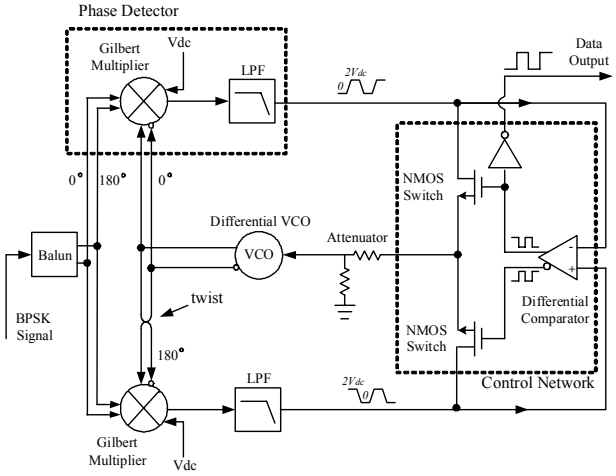

Fig. 1. Block diagram of the BPSK demodulator MMIC.

II. MMIC Coherent BPSK Demodulator

A block diagram of the novel anti-parallel-loop BPSK demodulator is presented in Fig. 1. It comprises an active balun, an anti-parallel dual loop, and a control network. The balun is to convert the received BPSK signal to the required differential signal for the double-balanced Gilbert-Cell phase detector. The dual loop after the balun contains two phase-locked loops (PLL) that share a differential VCO and are controlled by the control network. There is 180° phase difference between the two phase-locked loops, and thus the name "anti-parallel" dual loop. In one of our previous works [8] we demonstrated a proto-type of this circuit using low-frequency (i. e., baseband) packaged components. In this paper, we describe the unique monolithic implementation of the circuit at a microwave carrier frequency of 2.7 GHz.

The concept of this demodulator is that with a proper control of the two NMOS switches by the differential comparator in the control network, the anti-parallel dual loop with 180° phase difference can offer the locking to the received BPSK signal, in which the carrier signal also switches its phase by 180° in accordance with the data. For example, when the received BPSK signal is at 0° phase, the upper switch closes and the lower switch opens, and the detector output of the upper loop is fed to the VCO and the upper loop operates like a PLL (a locking loop) in this case. When the received BPSK signal switches its phase to 180°, the upper switch opens and the

lower switch closes, and thus the lower loop will operate as the locking loop.

To realize the above operations, the NMOS switches need two opposite control signals from the comparator. Generating these opposite signals requires a voltage difference between the two inputs to the comparator from the dual loop. As described in [8], two identical DC offset voltages V_{dc} are introduced to the phase detectors (by using two voltage summers after the multipliers) to differentiate their two outputs. In this manner, when the locking loop is locked, its multiplier's output (IF) has to be $-V_{dc}$, in order to cancel the introduced offset voltage V_{dc} at the summer. This will make the input signal to the VCO equal to 0 V, which is needed for locking. In the other loop, due to its 180° phase difference from the locking loop, its multiplier will output V_{dc}. After summing with the other introduced V_{dc}, its final output will be $2V_{dc}$, compared to the zero output of the first loop. This process works regardless of which of the two loops is in lock. The two different loop outputs enable the comparator to generate the proper control signals. When the input BPSK signal switches its phase by 180° difference, the two loop outputs will switch between 0 and $2V_{dc}$, and the differential comparator will also switch its two opposite outputs accordingly, as illustrated in Fig. 1. It can be noted that these outputs are actually the demodulated data. An inverter is placed after the comparator for the data output, as shown in Fig. 1.

The implementation details of the components in the demodulator MMIC are described next. Fig. 2 shows the schematic of the active balun. A common-gate (CG) NMOS T_1 and a common-source (CS) NMOS T_2 are used to convert the single-ended input signal to the differential signals, which is similar to the bi-phase splitter in [9]. The use of the CG configuration at the input has the advantage of broadband matching, which eliminates the need for an input-matching network for the received 2.7GHz BPSK signal. The voltage followers T_3 and T_4 are used for isolation between the CG-CS transistor stage and the dual PLL.

As shown in Fig. 1, after the balun the dual PLL consists of Gilbert-Cell phase detectors, low-pass filters (LPFs), and a differential VCO with a voltage attenuator for loop gain control. The differential signal paths from the VCO to the lower multiplier are twisted once, by which an 180° phase shift is easily produced and thus eliminates the use of any other phase shifting devices. This MMIC demodulator makes the best of this configuration to reduce the system complexity. Similar to a single PLL, the dual loop here also requires an optimum damping factor for its locking performance [5]:

$$\zeta = \sqrt{\omega_c / 4k_d k_o} = 1/\sqrt{2} \approx 0.707 \qquad (1)$$

where ω_c is the cutoff frequency of its loop filters (the LPFs), k_d is the phase detector gain, and k_o is the gain constant of the VCO. Among these three loop parameters, ω_c is determined by the data rate because the loop filters also work as the data filters, and k_d is designed to be large to let the phase detectors generate comparable outputs in order to drive the differential comparator. Therefore, k_o is selected to be adjusted here to achieve the optimal damping factor. The loop filters in this demodulator are realized with two RC low-pass filters for simplicity. Their cutoff frequency is designed to be 33MHz to allow a high data rate. The other loop components with their parameters (i.e. k_d and k_o) are discussed below.

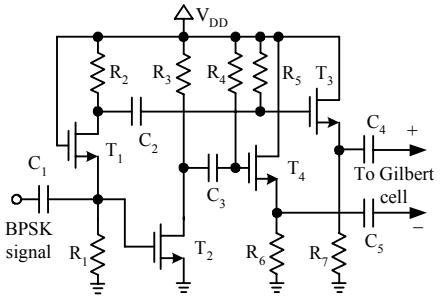

Fig. 2. The CG-CS active balun.

Gilbert-cell multipliers were chosen for the phase detectors. Their schematic is presented in Fig. 3 (T_5~T_{10}), where a DC offset is introduced to the multiplier's output by a differential-pair voltage summer (T_{11}~T_{14}). As a common mixer, the Gilbert cell has excellent isolation among its three signals LO, RF, and IF due to its balanced structure. Moreover, its active configuration can give the detectors a high gain. A detector gain of k_d=1.2 volt/rad is achieved in the simulation of this multiplier. The IF mixing product of the multiplier is then fed to the voltage summer, where the required DC offset is added into the IF mixing product by adjusting the control voltage V_C of its current mirror. The DC offset V_{dc} at the output of the voltage summer is related to V_C by

$$V_{dc} = V_{DD} - I_S R_{11}/2 = V_{DD} - (V_C - V_{SS})R_{11}/2R_C \qquad (2)$$

If the ratio of the resistors R_{11} and R_C is chosen to be 2 and V_{DD}=-V_{SS}, the expression in (2) can be simplified to

$$V_{dc} = -V_C \qquad (3)$$

Thus the output of the voltage summer will contain the IF mixing product from the multiplier and the DC voltage $-V_C$. The above analysis ignores the DC bias from the multiplier, which might need to be further compensated at the voltage summer by V_C. Since the dual loop requires two identical voltage summers, their current mirrors are combined to use just one control voltage (the transistor T_{14} in one voltage summer is eliminated). This combination

not only simplifies the circuitry, but also reduces the possibility of any mismatch between the two DC offsets. The current mirrors used for the tail currents in the multipliers are also combined in the same way to achieve symmetry between the two phase detectors.

A complementary cross-coupled topology is adopted to implement the differential VCO, as shown in Fig. 4. Its

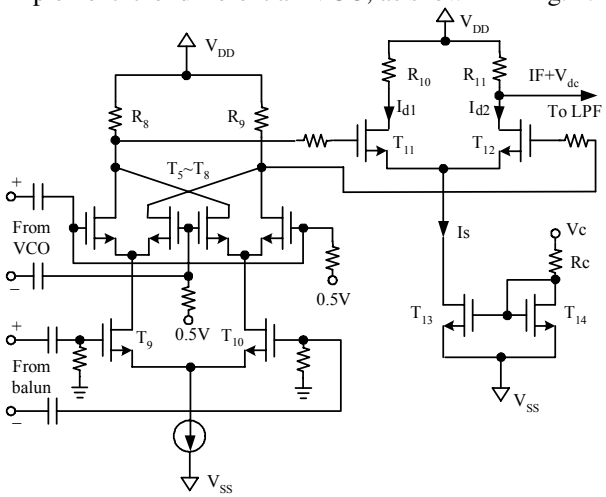

Fig. 3. The Gilbert-cell multiplier with a voltage summer.

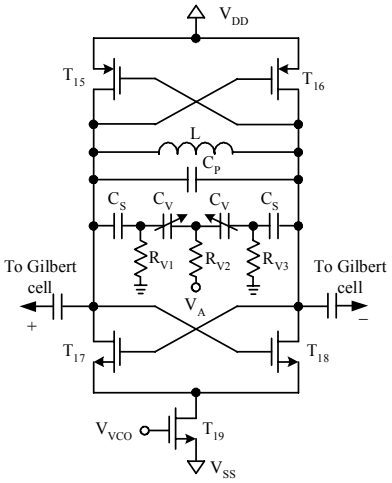

Fig. 4. The complementary differential VCO.

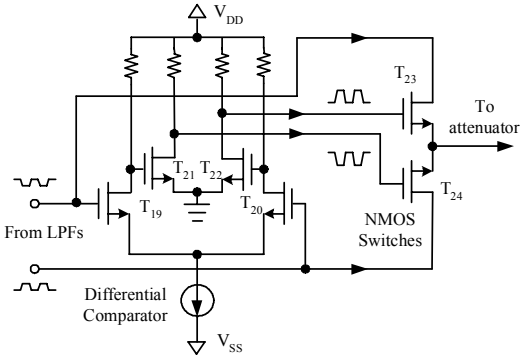

Fig. 5. The differential comparator and the two switches

gain is controlled through the bottom transistor T_{19}. The cross-coupled topology is preferred here due to its relatively good phase noise and ease of implementation [10]. An on-chip spiral inductor L (2 nH) and a MOS-varactor network compose the LC resonator for the VCO, which is designed to work at 2.7 GHz. The varactor network includes two identical varactors (C_V) biased by three high-value resistors R_{V1}~R_{V3}, two series capacitors C_S and one parallel capacitor C_P. The series capacitors (C_S) block any DC voltage from the transistors to make the frequency control independent from the gain control by T_{19}. The parallel capacitor C_P is introduced to reduce the varactors' tuning range versus their tuning voltage V_A, in order to lower the VCO's gain constant for the optimization purpose of the damping-factor in (1). With the cutoff frequency of the LPFs ($2\pi\times 33$ Mrad/sec) and the phase detector gain (1.2 volt/rad), a gain constant of 86 Mrad/sec/volt is selected for this VCO (including the voltage attenuator) to achieve the optimal damping factor. A large output of the VCO is not pursued in this demodulator because a large output could overdrive the Gilbert multipliers. This simplifies the other design issues of this VCO, such as its Q factor.

The control network in the demodulator controls the dual loop. It consists of two NMOS switches, a differential comparator, and an inverter for the data output. The differential comparator and the NMOS switches are presented in Fig. 5. Two single NMOS transistors (T_{23} and T_{24}) are used as the switches. Their control signals come from the differential comparator that contains a differential pair (T_{19}~T_{20}) and two common-source amplifiers (T_{21}~T_{22}). The differential pair and the two amplifiers are biased at their threshold regions to achieve high gain, and thus high sensitivity for this comparator.

The BPSK demodulator shown in Fig. 1 was implemented in an MMIC using the described components. Compared with the Costas loop demodulator [7] that is quite common in current communications receivers, the proposed demodulator eliminates the need for a 90° phase shift in the local oscillator, which would require either a phase shifter or a quadrature VCO. In either case, the result is the increased size and power consumption. Furthermore, the Costas loop demodulator requires a third multiplier and a third loop filter at the VCO input to correct the sign of the phase error from its locking loop [7], [11], [12]. The third loop filter not only increases the circuit size by its passive devices, but also introduces more delay. Equation (1) would have to be changed to include the effect of this third loop filter, which makes the design more complex. In the proposed demodulator, instead of the third multiplier and the third

loop filter, two NMOS switches and a differential comparator are used, which are more compact and easier to design. The Costas loop demodulator also requires a summer to combine its dual loop's outputs for its demodulated data [7], which is not required in the proposed demodulator.

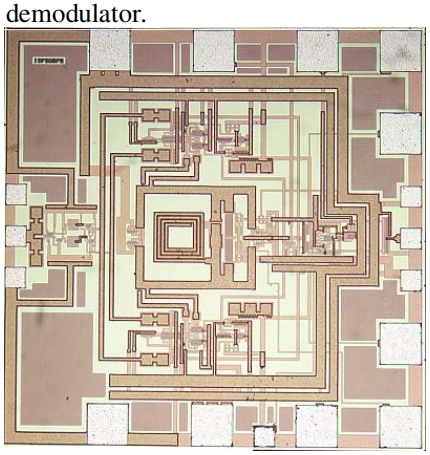

Fig. 6. The microphotograph of the fabricated BPSK demodulator MMIC under test

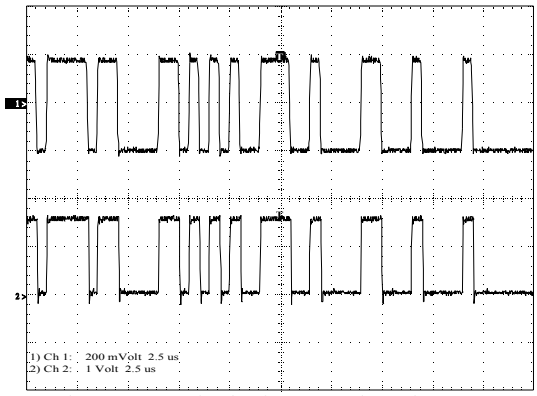

Fig. 7. The top trace is the input random data stream at the modulator and the bottom trace is the demodulated data using the anti-parallel synchronization loop. The data rate is 2 Mbps.

III. Measurement Results

The proposed coherent BPSK demodulator was fully integrated in an MMIC using 0.18 μm CMOS technology without any external passive components (e.g. inductor coils, capacitors, crystals). Fig. 6 shows a microphotograph of the fabricated demodulator MMIC under test. The whole demodulator system is compact and it measures 1 mm^2 including the bonding pads.

A BPSK signal was generated for the demodulator input using a commercial bi-phase BPSK modulator, in which a 2.7 GHz carrier signal was used along with a random data stream. The generated BPSK signal (-13.5dBm) was then fed to the demodulator MMIC for the demodulation test. The demodulation test was successful. Fig. 7 shows the measured random data carried on the received BPSK signal and the successfully demodulated data by the demodulator MMIC at a data rate of 2 Mbps. Comparison of the two data streams in the figure shows clearly that all the random data bits were demodulated properly. This demodulator MMIC was tested at data rates of up to 7Mbps and it performed quite well. The required minimum power of the input BPSK signal in the test is –20 dBm, which is the input sensitivity of this MMIC demodulator. The total DC power consumption of this MMIC demodulator is 151 mW.

IV. Conclusion

An MMIC coherent BPSK demodulator was successfully implemented based on our previously-proposed demodulator concept. Its compact structure and ease of implementation make it a good candidate for the potential applications in GPS receiver systems and RFID tag reader systems.

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