An L-band Direct-Digital QPSK Modulator in CMOS

Ahmed M. El-Gabaly*, Brad R. Jackson, and Carlos E. Saavedra
RF and Microwave Circuits Laboratory, Queen's University
19 Union St, Walter Light Hall
Kingston, ON K7L 3N6 Canada

***Abstract* — A new direct-digital Quadrature Phase Shift Keying (QPSK) modulator is proposed for portable wireless applications. Its compact yet effective design includes passive phase shifters, active baluns and pass transistors for low-power operation. The Integrated Circuit (IC) has been implemented in a low-cost 0.18um Complimentary Metal-Oxide Semiconductor (CMOS) process with a 1.8V supply. Experimental results at 1.7GHz show solid performance with the data transmission rate and carrier rejection exceeding 20Mbps and 40dB respectively.**

***Index Terms* —** Digital modulation, quadrature phase shift keying, CMOS integrated circuits, portable radio communication.

I. Introduction

The demand for inexpensive, light and low-power portable products such as cellular phones, digital cordless phones and wireless Local Area Networks (LANs) has been growing rapidly in recent years [1]. To meet this trend, much effort has been made in integrating the radio frequency (RF) front-end with digital circuits for reduced overall system size, cost and power. As CMOS is the dominant technology for digital circuitry, it is naturally suited for implementing such full system-on-chip (SoC) transceivers [1].

Modern wireless standards (IEEE 802.11b/g, DECT) employ complex vector modulation such as Quadrature Phase Shift Keying (QPSK) for increased spectrum efficiency and lower bit error rates. Such modulation schemes have been traditionally implemented using heterodyne modulators since it was difficult to design direct (RF) modulators with adequate accuracy [2]. However recent developments in high-speed monolithic technologies such as Complimentary Metal-Oxide Semiconductors (CMOS) make it now possible to manufacture direct RF modulators with improved performance, potentially leading to new wireless standards in the future.

Direct modulators have a number of advantages over their traditional heterodyne counterparts. For instance, they eliminate the need for multiple oscillators and high quality filters, greatly reducing the size of the system and facilitating integration with existing digital CMOS circuits. In addition, higher data transmission rates are possible since the signal bandwidth is no longer limited by the low intermediate frequency (IF) [3].

Several direct QPSK modulators have been reported in recent literature [1]-[6]. Most of these designs achieve quadrature modulation by using a pair of Gilbert mixers [1]-[3] and inductor-capacitor (LC) quadrature oscillators [4]-[5]. This approach significantly augments Integrated Circuit (IC) size, cost and power. Furthermore, the reported designs were only tested with random input data rates of a few Megabits per second (Mbps). Finally, more expensive technologies such as Gallium Arsenide (GaAs), Silicon Bipolar and BiCMOS were used to realize some of these circuits.

In this paper, a compact QPSK modulator capable of processing binary data directly, without any Digital-to-Analogue Converters (DACs), is proposed. It provides an inexpensive and low-power solution by using passive phase shifters, pass transistor circuits and active baluns. The experimental IC has been designed and fabricated in a low-cost 0.18um CMOS technology to consume only 43mW from a 1.8V supply. Measurements at 1.7GHz carrier frequency show good performance with data transmission rates and carrier rejections exceeding 20Mbps and 40dB respectively. This paper is organized as follows: Section II describes the principle operation and design of the circuit, Section III discusses the experimental results, and Section IV concludes the work.

II. Circuit Architecture and Design

A block diagram of the direct-digital QPSK modulator is shown in Fig. 1. It consists of: 1) a resistor-capacitor, capacitor-resistor (RC-CR) phase shifter; 2) two buffers; 3) two active (wideband) baluns; 4) two pairs of pass transistor switches; 5) a differential amplifier summing junction and 6) an output buffer.

In the phase shifter, two quadrature carriers with a 90° phase difference ($\cos(\omega t)$ and $\sin(\omega t)$) are created from the input RF signal. Each quadrature carrier is then split in the baluns into differential signals, yielding $\pm\cos(\omega t)$ and $\pm\sin(\omega t)$. One signal from each balanced quadrature pair, $\pm\cos(\omega t)$ and $\pm\sin(\omega t)$, is later selected in the pass transistor circuits according to the in-phase (I) and quadrature-phase (Q) data values respectively. Finally, the output signals are subtracted in a differential pair amplifier. In effect, the circuit implements the following QPSK function:

$$QPSK(t) = I(t)\cos(\omega t) - Q(t)\sin(\omega t), \quad (1)$$

where $I(t)$ and $Q(t)$ represent the I and Q bit streams in time with a value of +1 for logic 1 and -1 for logic 0. It is important to note that the arithmetic operation in (1) is merely inconsequential, i.e. either an addition or subtraction can be chosen as long as it is performed using complex vector arithmetic.

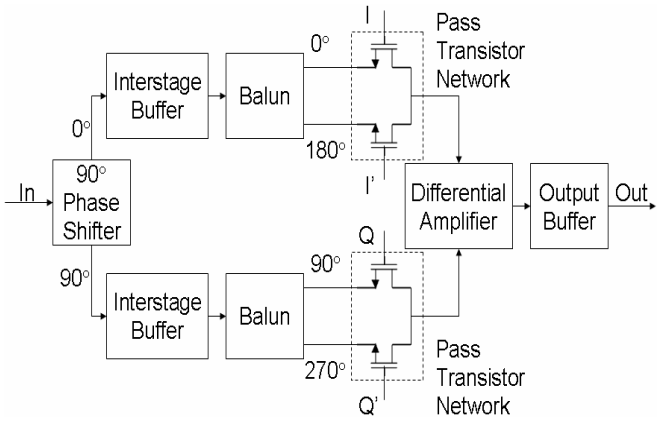

Fig. 1. Block diagram of proposed QPSK modulator.

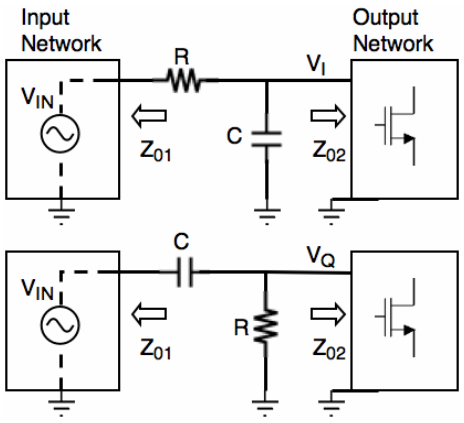

Fig. 2. Integrating and differentiating RC networks of the phase shifter.

A. Quadrature Phase Shifter

The RC-CR network is chosen for generating quadrature carriers due to its small footprint and zero DC power consumption. It is also useful for overcoming phase errors caused by fabrication tolerances as shown later. Fig. 2 [6] shows the integrating and differentiating RC circuits involved. In this figure, Z_{01} and Z_{02} are the impedances of the input and output networks, while R and C are the resistance and capacitance of the integrating and differentiating circuits. The outputs V_I and V_Q are given by [6]:

$$V_I = \frac{1}{\left(1+\frac{R}{Z_{02}}+\frac{Z_{01}}{Z_{02}}\right)+j\omega C\left(R+Z_{01}\right)} \tag{2}$$

$$V_Q = \frac{1}{\left(1+\frac{Z_{01}}{R}+\frac{Z_{01}}{Z_{02}}\right)+\frac{1}{j\omega C}\left(\frac{1}{R}+\frac{1}{Z_{02}}\right)}. \tag{3}$$

From (2) and (3) above it can be seen that the phase difference θ between the two outputs V_I and V_Q is not 90° due to the finite Z_{02}. However if $Z_{02} >> (R, Z_{01})$ then:

$$\begin{aligned}\theta &= \angle V_Q - \angle V_I \\ &\approx 90° - \tan^{-1}\left(\omega C\left(R+Z_{01}\right)\right) + \tan^{-1}\left(\omega C\left(R+Z_{01}\right)\right) \\ &= 90°\end{aligned} \tag{4}$$

as needed. The amplitude imbalance G in this case is:

$$G = \left|\frac{V_Q}{V_I}\right| \approx \omega C R\,. \tag{5}$$

.

Equation (4) shows that the phase difference is at a constant 90° with no frequency dependence. Also, it is independent of tolerances in resistance or capacitance values due to the fabrication process. However, from (5), amplitude balance is only achieved at the design carrier (cutoff) frequency of ω=1/(RC) [6].

B. Interstage Buffers

Buffers consisting of common-drain (source follower) devices present high output impedance to the preceding phase shifter for improved quadrature phase and amplitude matching. They are also necessary to sufficiently drive the following low input impedance baluns, which are discussed in the next section.

C. Wideband Baluns

Many active baluns have been reported in the literature to create 180° out-of-phase signals that are needed for a variety of applications including modulators and mixers. The most common active balun takes on the form of a differential pair or a common-source/common-gate pair [7]-[8].

A schematic of an active balun designed in previous work [9] and used here is shown in Fig. 3. It consists of a common-gate/common-source pair, with the common-gate device designed to provide a low input resistance (~$1/g_m$) for an impedance match and a lower reflection coefficient. This is achieved over a wide bandwidth without using any bulky matching networks. For more details on the balun, see [9] and its associated references.

D. Pass Transistors

The purpose of the I, Q pass transistor networks is to pass one signal from each quadrature complementary pair (±cos(ωt) and ±sin(ωt)), while blocking the other one. In particular, the in-phase signal cos(ωt) (sin(ωt)) is passed for a binary digit of I=1 (Q=1) while the out-of-phase signal -cos(ωt) (-sin(ωt)) is passed for I=0 (Q=0) thus creating the I(t)cos(ωt) (Q(t)sin(ωt)) product term in (1). The two selected quadrature carriers can be subtracted to generate the QPSK vector signal as shown in the next section.

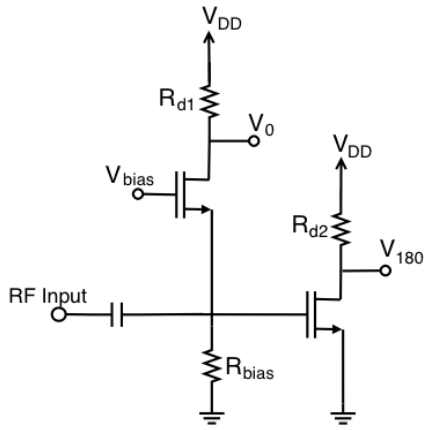

Fig. 3. Circuit schematic of active balun core.

Each pass transistor circuit consists of a pair of NMOS analog switches as shown in Fig. 1, which have the advantages of small footprint and low power consumption. Using the long-channel transistor approximation, the drain current-voltage (I_{DS}-V_{DS}) characteristic of an NMOS switch in the on-state (triode region) can be written as:

$$I_{DS} \approx k_n \frac{W}{L}(V_{GS} - V_T)V_{DS} . \quad (6)$$

It is clear from (6) that increasing the device width W would reduce the switch's on-resistance (V_{DS}/I_{DS}) and thus the signal loss across it. However doing so will also increase the gate-to-source parasitic capacitance ($C_{gs}=C_{ox}WL$) causing more coupling of the data signals (I and Q) to the output and hindering performance. So a trade-off is needed and a medium device size of 10 2.5um-wide fingers is used.

E. Differential Amplifier and Output Buffer

Fig. 4 shows the circuit schematic of the differential amplifier and output buffer. It contains only a few transistors and resistors making its size comparatively small and saving substantial IC space.

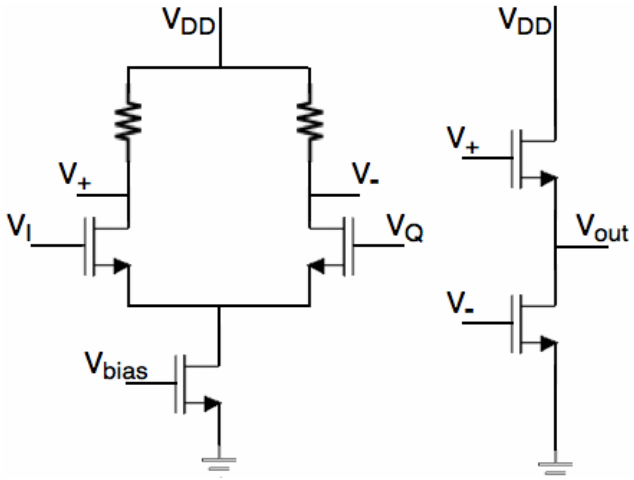

Fig. 4. Differential amplifier and output buffer circuits.

The differential amplifier subtracts the quadrature outputs of the pass transistor circuits (I(t)cos(ωt) and Q(t)sin(ωt)) and generates the resultant QPSK signal vector (QPSK(t)) as in (1). Fig. 5 below illustrates this vector subtraction process. Using a differential amplifier for vector subtraction eliminates the need for a passive structure, which would be prohibitively large at this frequency. The differential amplifier also eliminates traces of spurious signals and noise that are in common-mode. An output buffer of common-drain and common-source devices then converts the differential outputs to a single-ended one and drives the external 50Ω load with a low reflection coefficient.

III. Experimental Results

The QPSK modulator was fabricated in a standard (six-metal, single-poly) 0.18μm CMOS process. A photograph of the IC is shown in Fig. 6. It occupies a die area of about 0.425×0.850mm including bonding pads and consumes less than 43mW from a 1.8V supply.

A direct on-wafer measurement of the IC was carried out using co-planar RF probes and DC probes. RF and arbitrary function generators were used to apply the needed RF carriers and digital signals respectively.

The carrier rejection of the QPSK modulator was measured by applying the same square wave to both I and Q data channels. Fig. 7 is a plot of the output signal spectrum at 1.7GHz with a 0.5MHz square wave (1Mbps data rate), showing a carrier rejection of more than 40dB relative to the main lobes. This test was performed using a -20dBm input carrier level.

As the transmitted information in real systems is most often random as opposed to periodic, further tests were carried out. Pseudorandom binary sequences with a 9-bit shift register were employed to mimic random data. Fig. 8 shows the output signal spectrum at 1.7GHz with a data rate of 10Mbps per channel, for a total throughput of 10Mbps × 2 channels = 20Mbps. It is evident that this spectrum is the expected QPSK spectrum, featuring side lobes 17dB lower than the main one. It should be noted that all of these measurements were made without filtering any of the digital signals or the output of the IC.

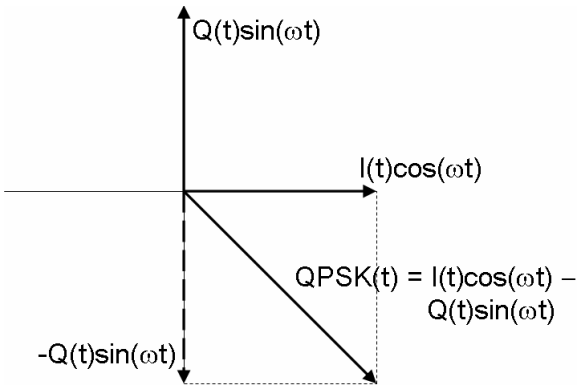

Fig. 5. Vector subtraction performed by differential amplifier.

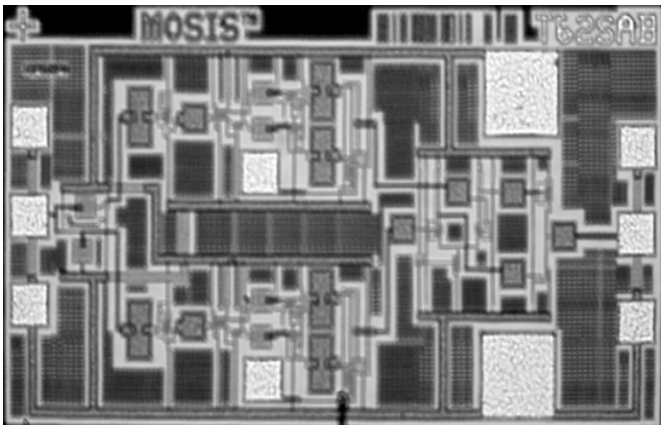

Fig. 6. Photograph of the QPSK modulator IC.

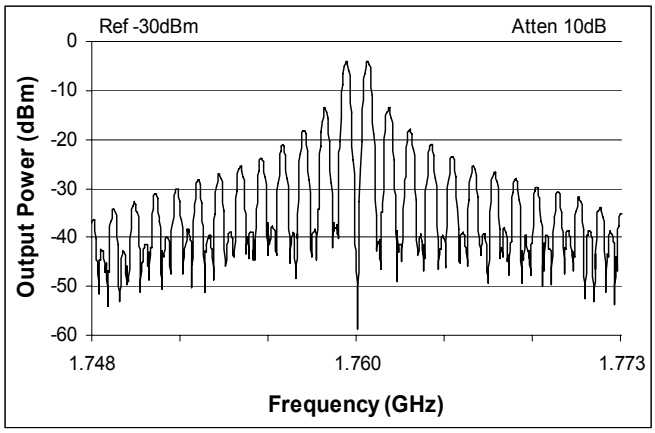

Fig. 7. Plot of the measured carrier rejection.

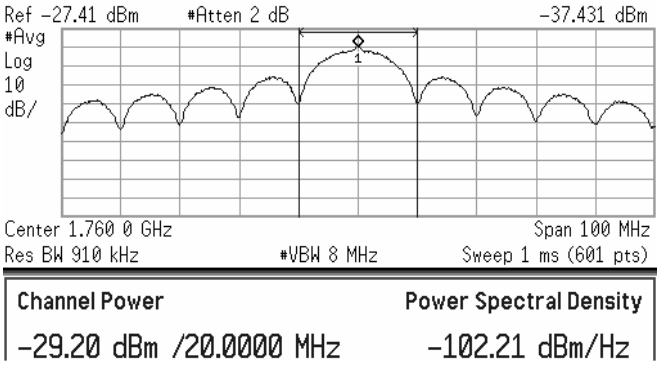

Fig. 8. Measured output QPSK spectrum at 20Mbps.

Table I summarizes the measured performance, including the input inferred 1dB compression point (P_{-1dB}).

IV. Conclusion

A compact QPSK modulator for portable wireless applications has been successfully developed using low-cost CMOS technology. The device generates the QPSK signal directly from digital data using a pair of pass transistor circuits and active baluns, thus consuming little power. Experimental measurements were presented at 1.7GHz showing good performance with high data transmission rates and carrier rejections of 20Mbps and 40dB respectively.

TABLE I
SUMMARY OF IC CHARACTERISTICS

Characteristic	Result
Die area (including pads)	0.425×0.850 mm
DC power	43mW from 1.8V
Data throughput	20Mbps (2×10Mbps)
Carrier rejection	>40dB
1dB Compression Point	+3dBm

Acknowledgment

The authors wish to thank the efforts of several colleagues in the RF and Microwave Circuits Laboratory at Queen's University for their contributions to circuit design and test. They would also like to acknowledge the Canadian Microelectronics Corporation (CMC) for their assistance in IC verification and fabrication.

References

[1] Yijun Zhou and Jiren Yuan, "A 1 GHz CMOS Current-Folded Direct Digital RF Quadrature Modulator," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 25-28, June 2005.

[2] T. Tsukahara, M. Ishikawa and M. Muraguchi, "A 2-V 2-GHz Si-Bipolar Direct-Conversion Quadrature Modulator," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 2, pp. 263-267, February 1996.

[3] A. Boveda, F. Ortigoso and J. Alonso, "A 0.7-3 GHz GaAs QPSK/QAM Direct Modulator," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 12, pp. 1340-1349, December 1993.

[4] C. Wu and H. Kao, "A 2-V Low-Power CMOS Direct-Conversion Quadrature Modulator with Integrated Quadrature Voltage-Controlled Oscillator and RF Amplifier for GHz RF Transmitter Applications," *IEEE Transactions on Circuits and Systems-II*, vol. 49, no.2, pp. 123-134, February 2002.

[5] T. Ou and C. Tzuang, "Direct Radio-Frequency Digital Angle Modulator," *IEEE Electronic Letters*, vol. 39, no. 7, pp. 594-595, April 2003.

[6] K. Yamamoto, K. Maemura, N. Andoh and Y. Mitsui, "A 1.9-GHz-Band GaAs Direct-Quadrature Modulator IC with a Phase Shifter," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 10, pp. 994-1000, October 1993.

[7] J. Lin, C. Zelley, O. Boric-Lubecke, P. Gould, and R. Yan, "A Silicon MMIC Active Balun/Buffer Amplifier with High Linearity and Low Residual Phase Noise," *IEEE MTT-S Digest*, vol. 3, pp. 1289-1292, June 2000.

[8] M. Kawashima, T.Nakagawa, and K.Araki, "A Novel Broadband Active Balun," *33rd European Microwave Conference*, vol. 2, pp. 495-498, October 2003.

[9] C. E. Saavedra and B. R. Jackson, "Voltage-Variable Attenuator MMIC using Phase Cancellation," *IEE Proceedings Circuits, Devices, and Systems*, vol. 153, no. 5, pp. 442-446, October 2006.