A 3 GHz CMOS Quadrature Oscillator Using Active Superharmonic Coupling

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***Abstract* — A 3 GHz quadrature oscillator has been designed, fabricated, and measured using CMOS 0.18 µm technology. The oscillator uses an active superharmonic coupling technique to generate the quadrature signals. By using two identical LC differential oscillators with a 180° relationship enforced between the second-order harmonics that are present at the common-mode nodes, quadrature outputs are obtained at the fundamental frequency. Quadrature oscillations were achieved at 3.0 GHz with a measured output power of -6 dBm. The phase error in the fundamental quadrature outputs is less than 6° and the power consumption for the core of the oscillator is 7.5 mW. The phase noise performance is -116 dBc/Hz at a 1 MHz offset and the figure of merit is -177 dBc/Hz. The layout for this circuit is very compact at 650 µm x 500 µm.**

***Index Terms* — CMOS analog integrated circuits, Microwave FET oscillators, MMICs, RF CMOS, Superharmonic coupling, Quadrature oscillators.**

I. Introduction

Communication systems that use phase shift keying modulation frequently require a pair of local oscillator (LO) signals that are in quadrature, or 90° out-of-phase. Furthermore, quadrature signals are commonly required in direct-conversion receivers or low-IF systems as well as in digital radio communication systems such as GSM and DECT [1].

There are several techniques that can be employed to generate quadrature signals. One straight-forward method is to use an RC-CR phase shift network with a standard oscillator to create a 90° phase shift [2]. Since the phase shift is completely dependent on the values of the resistors and capacitors, any deviation in the fabricated values of these components will directly lead to a phase error. Resistors in particular have large tolerances in most CMOS processes, and therefore this method can lead to poor accuracy in the quadrature signals that are generated. Another approach to generate quadrature signals is to use a digital frequency divider that follows an oscillator running at twice the fundamental frequency [3]. The use of this technique at high frequencies is inherently limited since an oscillator operating at double the desired frequency is required. A third common technique is to force two VCOs to run in quadrature by using coupling transistors working at the fundamental frequency [4]. This technique suffers from a trade-off between quadrature accuracy and phase noise due to the effects of the coupling circuit on the oscillation frequency. To avoid this problem, a quadrature oscillator can be realized using superharmonic coupling. As illustrated in Fig. 1a, by employing differential coupling at the common-mode nodes where the second harmonic is predominant, quadrature signals are generated at the fundamental frequency. To implement the coupling of the second harmonic with a 180° phase shift, an inverting on-chip transformer has been used [5]-[7] (Fig. 1b). However, on-chip transformers consume a significant area on-chip and have a limited Q-factor, particularly in CMOS technology.

Recently, a method of replacing the inverting transformer with a cross-coupled differential pair was proposed [8] (Fig. 1c), which can significantly reduce the required chip area. In [8], a quadrature voltage controlled oscillator was designed in SiGe technology at 6 GHz and a phase noise of -105.8 dBc/Hz was measured at a 1 MHz offset. In this work, active superharmonic coupling was used to design a 3.0 GHz quadrature oscillator in CMOS 0.18 µm technology with improved phase noise performance and reduced layout area.

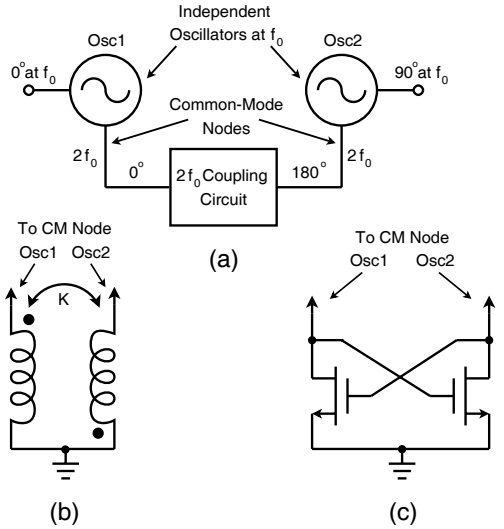

Fig. 1 (a) Superharmonic coupling of the second harmonic to enforce quadrature at the fundamental. (b) Coupling using an inverting transformer. (c) Coupling using a cross-coupled pair.

II. Circuit Design

The presence of harmonics in CMOS oscillator circuits is unavoidable. These harmonics are generally unwanted signals that appear with the desired fundamental signal. In differential oscillators there exist common-mode nodes (like the two source nodes in a cross-coupled oscillator) where higher-order harmonics are present and the fundamental is essentially absent. In fact, the second harmonic is usually dominant at these common-mode nodes, which makes them ideal locations to connect the inverting $2f_0$ coupling circuit. The performance of a quadrature oscillator using the superharmonic coupling topology will be determined by the performance of the two individual differential oscillators as well as the coupling network that enforces the anti-phase relationship between the second-order harmonics at the common-mode nodes.

One very common way of implementing a CMOS differential LC oscillator is to use a cross-coupled pair to generate the negative resistance required to overcome the losses in the tank. The resistance looking into the cross-coupled pair is given by $-2/g_m$ where g_m is the transconductance of each of the FETs in the cross-coupled pair. Therefore, with an appropriate device size and biasing, the negative resistance required to counteract the losses in the tank can be realized.

The complete quadrature oscillator circuit investigated in this work is shown in Fig. 2. It consists of two cross-coupled oscillators connected through a cross-coupled pair. It has been shown that by including cross-coupled PMOS transistors above the cross-coupled NMOS transistors the phase noise of the oscillator can be improved significantly due to the higher transconductance and faster switching speed of the complementary structure [9]. The oscillation frequency for each oscillator can be found from the familiar formula for the resonant frequency of an LC tank, $f_0=(2\pi\sqrt{LC})^{-1}$ where L is the value of the on-chip spiral inductor and C is the total capacitance at the tank nodes. The inductors used in this circuit were 150 μm x 150 μm with 4.25 turns. An electromagnetic simulation of this inductor geometry predicted an inductance of 2 nH and a Q-factor of approximately 4 at 3.0 GHz. The total capacitance including the lumped capacitor as well as the parasitic capacitance was 1.4 pF to provide oscillation at 3.0 GHz.

The network used to enforce the 180° phase difference in the second-order harmonics is a critical part of the quadrature oscillator. It is this anti-phase relationship that creates the quadrature phase relationship at the fundamental frequency. Convenient common-mode nodes for coupling the second harmonic are the common-source nodes in each cross-coupled differential pairs, shown as CM1 and CM2 in Fig. 2. DC blocking capacitors were used so that transistors N5-N6 could be biased for optimal coupling. Since any practical use of an oscillator involves connecting its output to other circuitry, buffers must be used to ensure that loading does not disrupt the oscillations. Source-follower buffers were used for each of the four outputs so that the oscillator can be measured using equipment with 50 Ω input impedances. The current sources shown in the buffer circuits in Fig. 2 were implemented with the common current-mirror configuration. The 180° and 270° outputs were terminated on-chip with 50 Ω loads and the 0° and 90° were connected to CPW pads for on-chip probing.

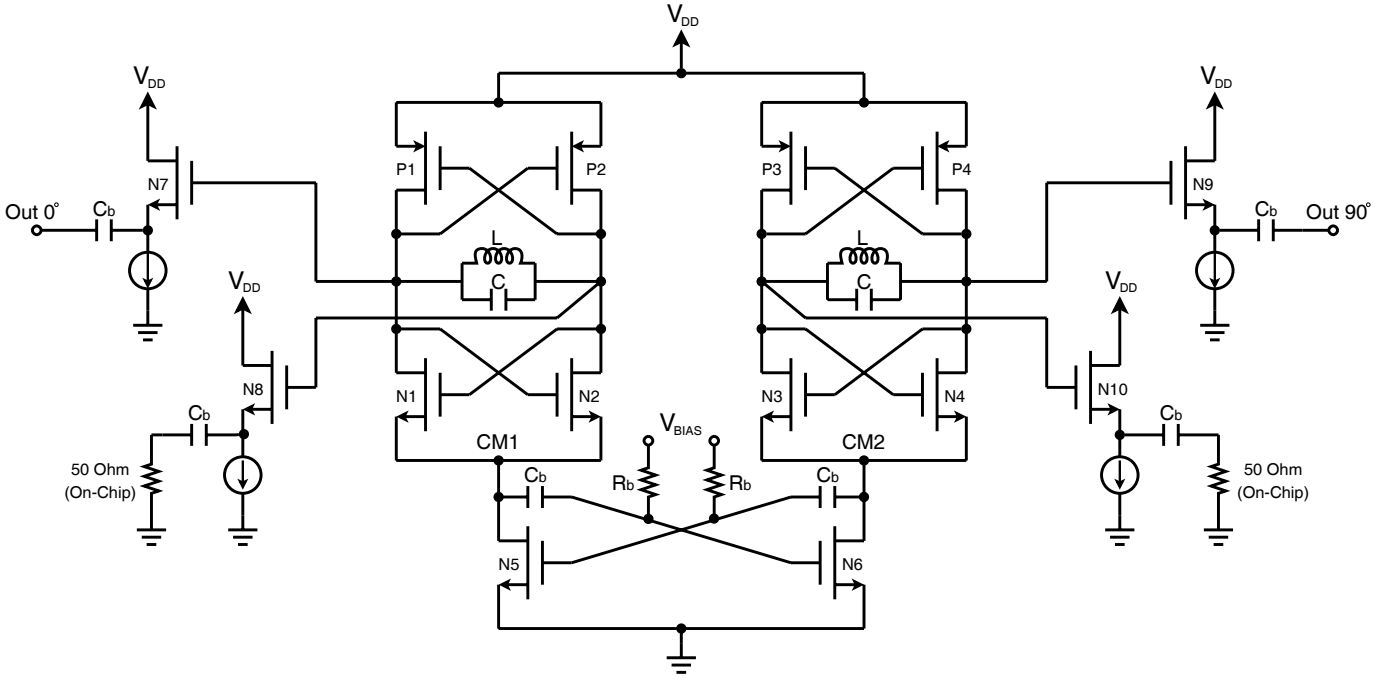

Fig. 2 Quadrature oscillator circuit using active superharmonic coupling.

III. Measurement Results

To characterize the quadrature oscillator chip, co-planar waveguide probes were used and several measurements were performed. The DC supply voltage was set to 1.8 V and the bias voltage for the coupling circuit, V_{BIAS}, was set to 0.85 V. To verify that the circuit is producing outputs that have a 90° mutual phase shift, a digital sampling oscilloscope (Tektronix TDS8000) was used. The test setup for this measurement is shown in Fig. 3. As shown in this figure, one output of the oscillator is split in order to generate the trigger signal for the oscilloscope with the other splitter output connected to Channel 1. An identical splitter is used in the other path with one output terminated in a 50 Ω load and the other splitter output connected to the Channel 2 input of the oscilloscope. This setup is used in order to maintain the phase and amplitude relationships between the oscillator outputs while also generating the required trigger signal. The loss and phase error introduced by the cables and splitters was measured using a vector network analyzer (Agilent 8510C). Shown in Fig. 4 are the time-domain output waveforms compensated for the loss and phase shift due to the measurement setup. The phase error was determined to be less than 6°.

To view the spectrum of the output signal, one of the quadrature oscillator outputs was connect to a spectrum analyzer (Agilent E4446A PSA) while the other output was terminated in a 50 Ω load. The resulting spectrum is shown in Fig. 5. The strongest spectral component is at 3.007 GHz with a power of approximately -6 dBm. The second harmonic at 6 GHz is below -20 dBc from the fundamental. The phase noise of the oscillator was also measured using the spectrum analyzer and the results are shown in Fig. 6. The phase noise at 100 kHz, 1 MHz, and 10 MHz offsets are approximately -90 dBc/Hz, -116 dBc/Hz, and -134 dBc/Hz, respectively. A commonly used figure of merit for oscillators is defined as [10]:

$$FOM = L(\Delta f) - 20log\left(\frac{f_c}{\Delta f}\right) + 10log(P_{DC})$$

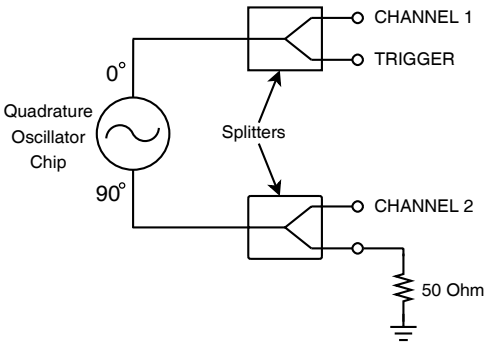

Fig. 3 Measurement setup for digital sampling oscilloscope.

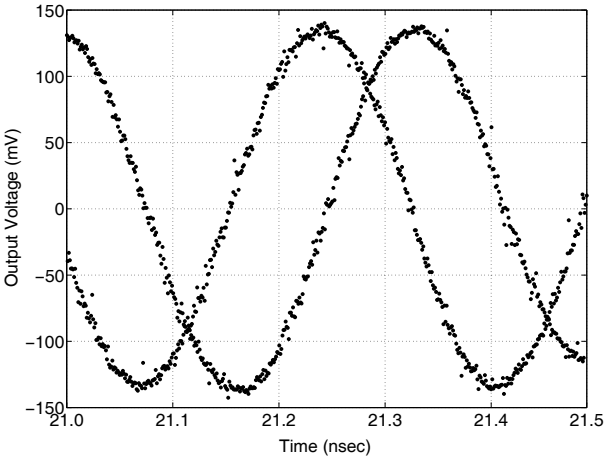

Fig. 4 Time-domain oscillator outputs.

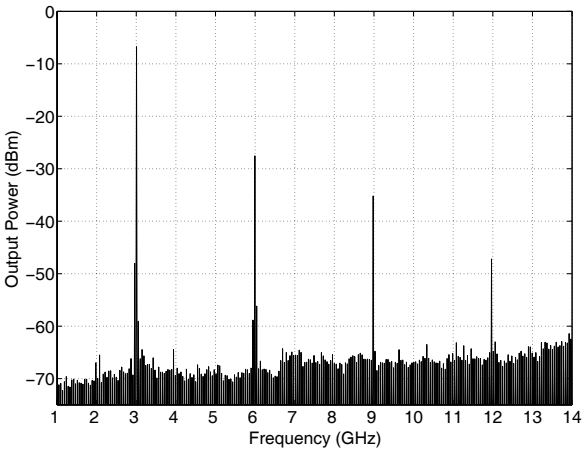

Fig. 5 Oscillator output spectrum.

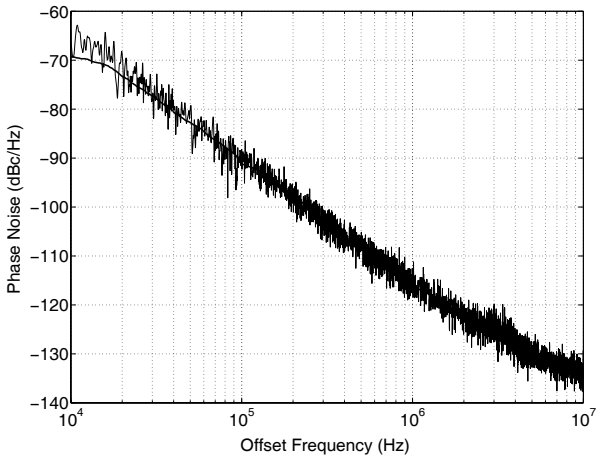

Fig. 6 Measured oscillator phase noise.

where f_c is the frequency of oscillation, Δf is the offset frequency, $L(\Delta f)$ is the phase noise in *dBc/Hz* at Δf, and P_{DC} is the power consumption in *mW*. The power consumption of the core of the quadrature oscillator is 7.5 mW (34 mW including buffers). Therefore, the figure of merit for this oscillator is -177 dBc/Hz at a 1 MHz offset. This result compares favourably with the VCO in [8], which uses a similar superharmonic coupling circuit and has an FOM of -170 dBc/Hz. Aided by the use of the use of a complementary cross-coupled topology, an improved phase noise and figure of merit were achieved in this work compared to the oscillator in [8] despite having a lower tank Q-factor in each oscillator. While better phase noise performance has been obtained with the use of a passive inverting transformer in [5]-[7], it comes at the cost of the significantly increased chip area required with that technique. The proposed CMOS quadrature oscillator in this paper has an area of 650 µm x 500 µm excluding pads and 800 µm x 670 µm including pads. This area is only 27% of the area used in [5] (2000 µm x 1000 µm) and 34% of the area used in [6] (1250 µm x 1250 µm), which both use superharmonic coupling with inverting transformers. The layout area is 83% of area used in [8], which introduced this active superharmonic coupling topology. A micro-photograph of the chip is shown in Fig. 7.

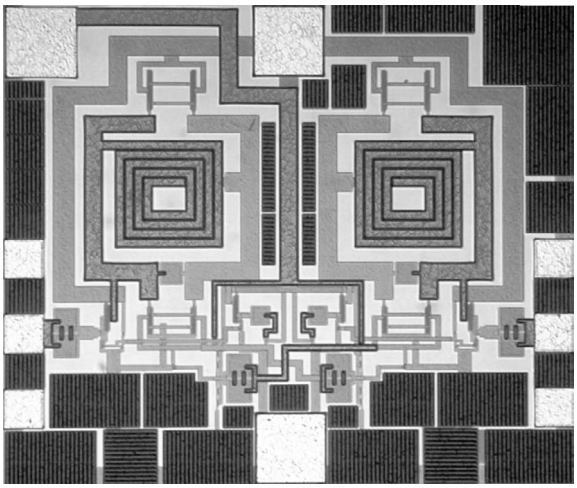

Fig. 7 Micro-photograph of the CMOS quadrature oscillator.

IV. Conclusion

A CMOS quadrature oscillator was designed at 3.0 GHz using superharmonic coupling. This technique couples the second-order harmonics between two oscillators and forces an anti-phase relationship, which in turn forces a quadrature relationship at the fundamental. To perform this coupling with a 180° phase shift, a cross-coupled differential NMOS pair was used at the common-mode nodes. A pair of cross-coupled PMOS transistors were used in each of the oscillator circuits in order to reduce phase noise. This circuit could easily be adapted to a VCO by simply replacing the lumped capacitors in the tank circuits with varactors.

This CMOS quadrature oscillator using active superharmonic coupling shows very good performance with an output power of -6 dBm, phase noise of -116 dBc/Hz at a 1 MHz offset, and a figure of merit of -177 dBc/Hz. Furthermore, by using a cross-coupled differential pair as opposed to an inverting transformer to create the 180° phase shift in the second-order harmonics, significant chip area and design time can be saved (since EM simulations of a passive on-chip inverting transformer are not necessary).

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