An L-Band CMOS Frequency Doubler using a Time-Delay Technique

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***Abstract* — In this paper, a frequency doubler circuit is presented that converts a 0.6 GHz signal to a 1.2 GHz output using standard CMOS 0.18 µm technology. The proposed circuit uses a time-delay element and an XOR logic gate to perform the frequency multiplication and is implemented entirely on-chip. Advantages of this topology include good fundamental suppression, compact layout, and low power consumption. Experimental results show a relatively constant output power of approximately 4 dBm with an input power from -3 dBm to 10 dBm, fundamental and third order harmonic suppressions of up to -30 dBc and a power consumption of 9 mW. The phase noise of the output signal is -117 dBc at a 500 kHz offset.**

***Index Terms* — CMOS frequency doubler, multiplier, mixer, frequency conversion.**

I. Introduction

Frequency multiplier circuits are used in a wide range of applications in communication systems. Using frequency multiplication, oscillators can be designed at lower frequencies and then converted to higher ones, which can simplify the design of the oscillator and improve the phase noise of the resulting signal.

Many CMOS frequency doubler circuits have been demonstrated using various methods [1]-[5]. A common technique is to use the non-linearities of a transistor with a large input signal such as in [2]. With this method, the output has many spectral components, among which is the desired doubled frequency signal. Input matching at the fundamental frequency is generally used, along with filtering and matching for the doubled frequency component at the output. An alternative frequency doubler circuit was proposed in [1] and demonstrated at baseband frequencies. That topology can also be employed monolithically and at much higher frequencies. Shown in Figure 1 is a block diagram and waveforms that describe the principle behind the frequency multiplication in this paper.

An input square wave, V_{in}, is delayed by T/4 where T is the input signal period, and is fed into an XOR gate along with the input. The output is a square wave with twice the frequency of the input. To implement the T/4 delay element, an integrator circuit is used along with a comparator. The integrator converts the square wave to a triangular wave and the comparator is then used to compare the triangular wave with a reference voltage. The result is V_d, a square wave that is delayed by T/4 with respect to the input. This signal is then used as the second input to the XOR gate to generate the doubled frequency at the output.

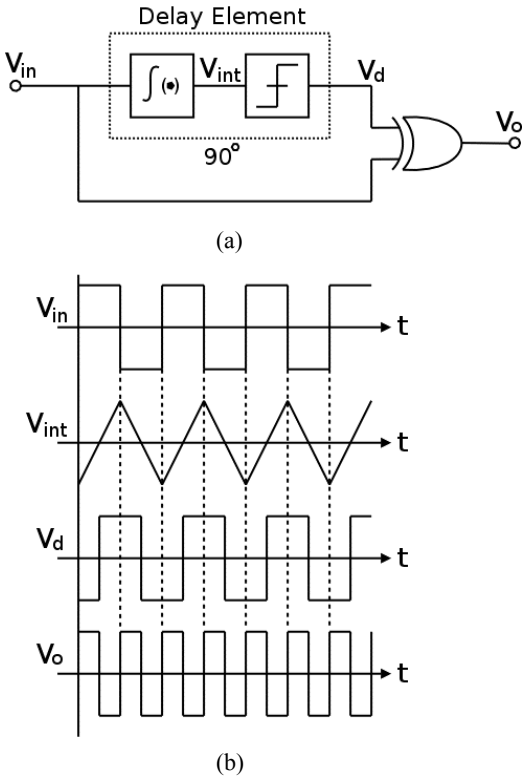

Figure 1 (a) Frequency doubler block diagram and (b) Waveforms

This topology can also be used as an analog multiplier by inputting a sinusoid, converting it to a square wave, and then filtering the odd-order harmonics of the square wave at the output.

In this paper, a 0.6 GHz to 1.2 GHz CMOS frequency doubler is presented based on the approach in Figure 1 and experimental results are shown. Using this technique, frequency multiplication can be achieved with low power consumption, small chip area, and good inherent rejection of undesired frequency components. In particular, a

significant advantage to this topology is that excellent fundamental suppression can be achieved at the output without filtering.

II. Circuit Design

A simplified schematic of the frequency doubler circuit is shown in Figure 2. Since the input to the circuit is a sinusoid and the doubler circuit requires a square wave, the first step is to make this conversion. To do this, a DC-level shifting circuit was used, followed by a series of inverters. The DC level shifting circuit offsets the incoming signal to the threshold voltage of the inverters. The inverters then create a high quality square wave for the core doubler circuitry.

The integrator was implemented using a passive RC integrator. The RC network approximates an ideal integrator when the period of the input signal is small with respect to the RC time constant. Note, however, that as the RC integrator becomes closer to an ideal integrator the amplitude of its output triangular wave becomes smaller and it consequently becomes more difficult for the comparator in the next stage to determine the correct state.

To implement the comparator circuit, first a common-source amplifier is used to amplify the triangular wave and then an inverter is used. Using this configuration for the comparator adds a small additional delay to the T/4 and as such could not be used at higher frequencies where this delay becomes significant.

The XOR gate was constructed using transmission gates [7] and inverters as shown in Figure 2. The output of this circuit is a square wave at twice the frequency of the input. If a sinusoidal output is desired, a simple low pass filter could be used to attenuate the higher order harmonics in the square wave. The layout for this circuit can be quite compact and in this implementation required an area of approximately 200 μm x 75 μm (0.015 mm^2) for the core of the frequency doubler circuit. The full chip area was 400 μm x 400 μm including bonding pads.

III. Experimental Results

To measure the performance of the proposed frequency doubler, an input sinusoidal signal at 0.6 GHz was used. The input power levels were varied and the output spectrum was observed. Shown in Figure 3 is the output spectrum with an input power of 4 dBm. The desired signal at 1.2 GHz is at approximately 4 dBm and is clearly the strongest at more than 30 dB above the fundamental at 0.6 GHz and the third harmonic at 1.8 GHz. The fourth harmonic at 2.4 GHz is approximately 14 dB below the 1.2 GHz signal. The presence of this harmonic is due to the uneven duty cycle of the output square wave which is caused by the two signals entering the XOR gate not being exactly 90° out of phase. To avoid this, the passive RC integrator could be adjusted, or a more sophisticated high speed comparator could be employed. Since this signal is 1.2 GHz away from the desired signal and already 10 to

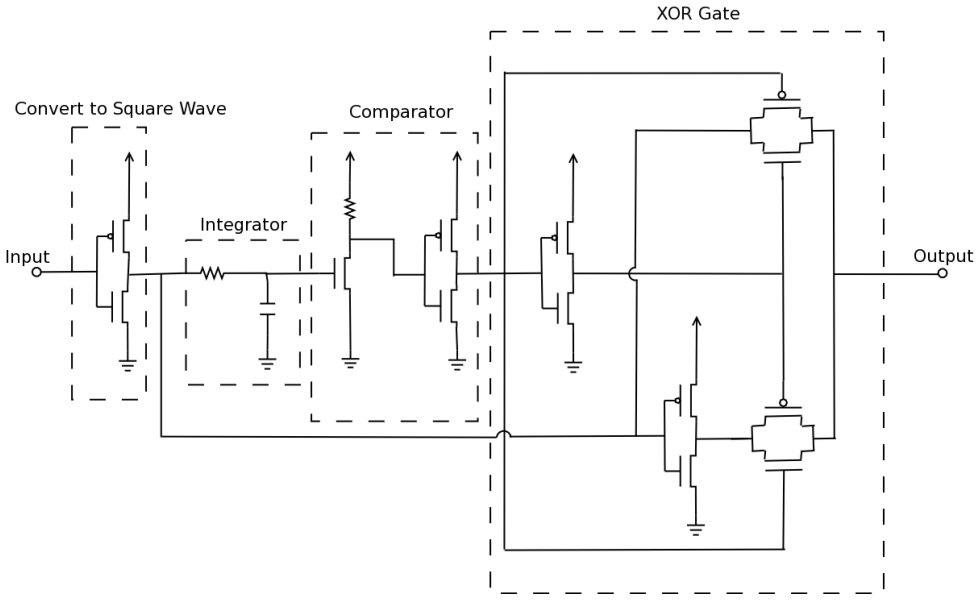

Figure 2 Simplified circuit diagram of the frequency doubler

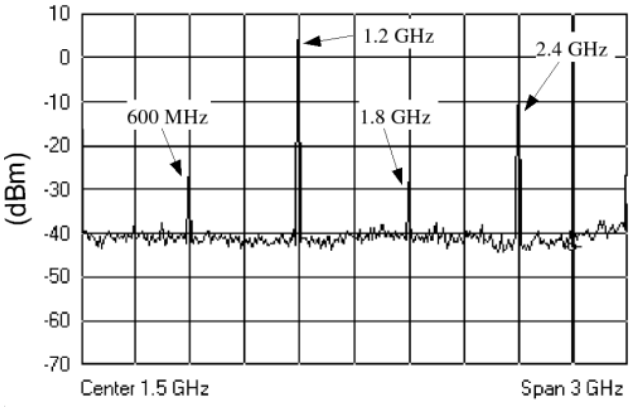

Figure 3 Output spectrum from 0 – 3 GHz with 4 dBm input power at 0.6 GHz

15 dB below it, it could easily be removed by filtering. Furthermore, since the output is a square wave, there are odd-order harmonics also present which could be easily filtered if a sinusoid is desired.

Shown in Figure 4 are the fundamental, second, third, and fourth harmonics at various input powers. It is apparent that the power of the frequency-doubled signal is relatively constant at approximately 4 dBm for input powers greater than -10 dBm. This constant output power is expected because of the digital circuit components with logic gates functioning from rail-to-rail producing a constant amplitude square wave at the output. At input powers higher than 0 dBm the fundamental and the fourth harmonic are significantly rejected and the third harmonic is at least 10 dB below the desired signal because the input is strong enough to generate a high quality square wave after propagating through the series of input inverters. At power levels below approximately -3 dBm the inverters at

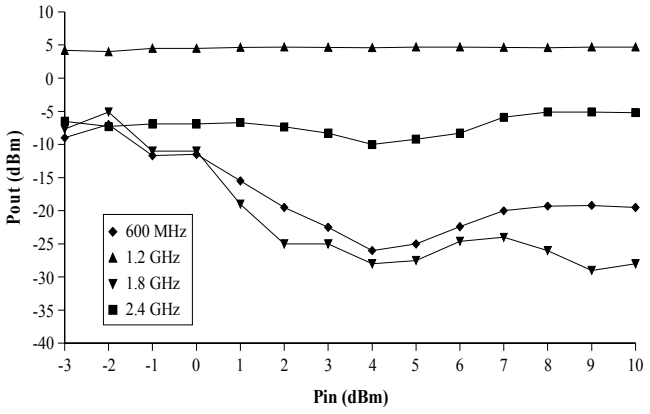

Figure 4 Harmonic output power levels with 0.6 GHz input signal

the input do not produce a well-defined square wave. Consequently, in this low input power region the second harmonic signal strength is close to that of the fundamental and other harmonics, thus the circuit is out of its operational range.

The phase noise of the 1.2 GHz output signal was measured to be -109 dBc at a 100 kHz offset and -117 dBc at a 500 kHz offset. The DC voltage used to power the circuit (Vdd) is 1.8 V and the circuit's DC current draw is 5 mA, resulting in a power consumption 9 mW for the circuit. A microphotograph of the chip is shown in Figure 5.

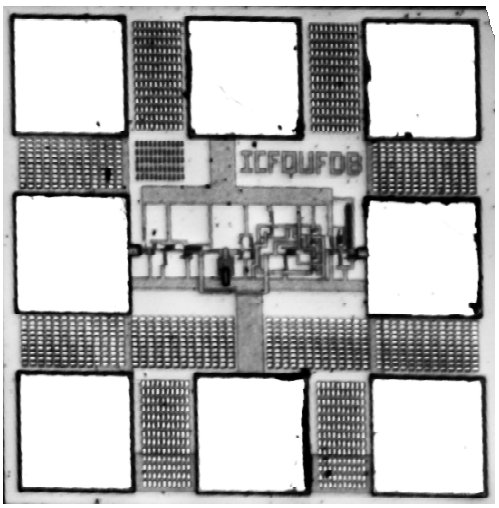

Figure 5 Microphotograph of the frequency doubler chip

IV. Conclusions

A microwave CMOS 0.18 μm frequency doubler circuit has been designed using a time-delay element, comparator and XOR gate. This circuit converts a 0.6 GHz input to a 1.2 GHz output. Experimental results show very good fundamental and third order harmonic suppression. A further advantage of this topology is the relatively constant output power of approximately 4 dBm over a wide range of input power levels. The power consumption of the circuit is 9 mW and the core circuit layout area is approximately 0.015 mm^2. This circuit could either be used as an analog multiplier by employing a low-pass filter to suppress the higher order harmonics of the output square wave or as a clock frequency doubler.

ACKNOWLEDGEMENTS

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