COMPACT CMOS VCO USING A TRANSISTOR FOR FREQUENCY CONTROL

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Abstract - **A compact CMOS voltage-controlled relaxation oscillator circuit is presented in this paper. The frequency control is fulfilled by using a single MOSFET to control the charging and discharging currents of a timing capacitor. This paper investigates and demonstrates the proposed control mechanism. The proposed VCO was fabricated using 0.18 μm CMOS technology and the fabricated VCO has a compact core size of only 80μm x 200μm, or 0.016mm^2. A linear tuning range from 650 MHz to 840 MHz, or a 28% range was achieved by the single MOSFET's control from a 1.8V DC supply voltage. The output power was –14.5 dBm with only ±1 dB variation in this tuning range. The corresponding power consumption was measured to be 5.4mW. Moreover, the VCO free-running frequency can be increased beyond 1.1 GHz by using higher DC supply.**

I. INTRODUCTION

Voltage controlled oscillators (VCOs) are key elements in wireless communication systems, in which they are employed in various phase-locked loops (PLL) to recover the RF carriers from different modulation-format signals [1]. They also have been widely used for the frequency synthesis in the signal generators [1][2]. There exist two concepts to control the frequency of a VCO. One is the varactor-control method in the LC-based VCOs and the other is the current-control method in the relaxation-based VCOs [3]. The relaxation-based VCOs are known for their wide tuning range [4]. The other advantage of the relaxation-based VCO is their compact size in the IC implementation, due to the fact that they avoid the use of the inductor. The on-chip inductor usually takes a large space in LC-based VCOs. While it is generally known that the phase-noise of the relaxation-based VCOs is higher than that of the LC-based VCOs [4], this phase-noise problem with the relaxation-based VCOs can be alleviated when they are applied in the PLLs and locked to the external low-noise reference sources, as adopted already in most frequency synthesizers [1][2].

Capacitor-current tuning through operational trans-conductance amplifiers (OTA) was developed for the frequency control of relaxation-based VCOs in [3] and [5]. In the relaxation-based VCO described in [3] (where it was called voltage-controlled multivibrator), an OTA output was connected to a capacitor, which was followed by a comparator with a feedback network. The charge/discharge operation of the capacitor was controlled by the comparator and its feedback network, while the charge/discharge time was determined by the OTA's transconductance. This transconductance was controlled by its DC bias current, resulting in a flexible frequency control mechanism. The relaxation-based VCO developed in [5] was similar to the one in [3], except that [5] applied a switching control on the OTA's DC bias current for the purpose of linear frequency control. Obviously the common problems with these two methods are the design complexity and difficulty of the OTA and the comparator. The maximal frequency of this type of VCO highly depends on the speeds of these two components, and is limited to several MHz [3].

Several other methods, such as emitter-coupled/source-coupled topologies [6][7] and double cross-coupled topologies [4][8], were also proposed later to implement high speed relaxation-based VCOs. The emitter-coupled topology [6] utilized a differential-amplifier-type circuit, with its two emitters capacitively coupled and its two outputs cross-fed to its two inputs via two voltage followers. The frequency control of such VCO was realized through the DC currents of the emitters. Due to the significant decrease of the complexity and the parasitics, this topology is able to achieve higher speed than the aforementioned OTA/comparator-based topology and is suitable for implementation at microwave frequencies. Moreover, low-phase-noise performance can be obtained by the capacitively emitter-coupling structure, which makes it more attractive. It has become an industry standard and the basis of the other topologies [4][7][8].

The CMOS topology for LC-based oscillators has been already analyzed in [9] to have the superiority over the all-NMOS topology, due to its higher transconductance and its symmetric output rise/fall time. There were, however, very few works investigating on a CMOS topology for the relaxation-based VCOs. A CMOS relaxation-based VCO using a single transistor for the frequency control is proposed and studied in this paper. It can result in a compact VCO with broad tuning range and low power consumption. The rest of this paper is organized as follows. Section II describes the operation of the proposed VCO and Section III is dedicated to the analysis of the frequency control of the proposed VCO. The measurement results of the fabricated VCO are presented in section IV. Section V concludes this work.

II. CIRCUIT DESCRIPTION

A schematic diagram of the proposed VCO is shown in Fig. 1. It contains a VCO core and an output buffer circuit. If the PMOSFET, T_C, and the resistor R_3 were removed from Fig. 1, the VCO core would work as a symmetric

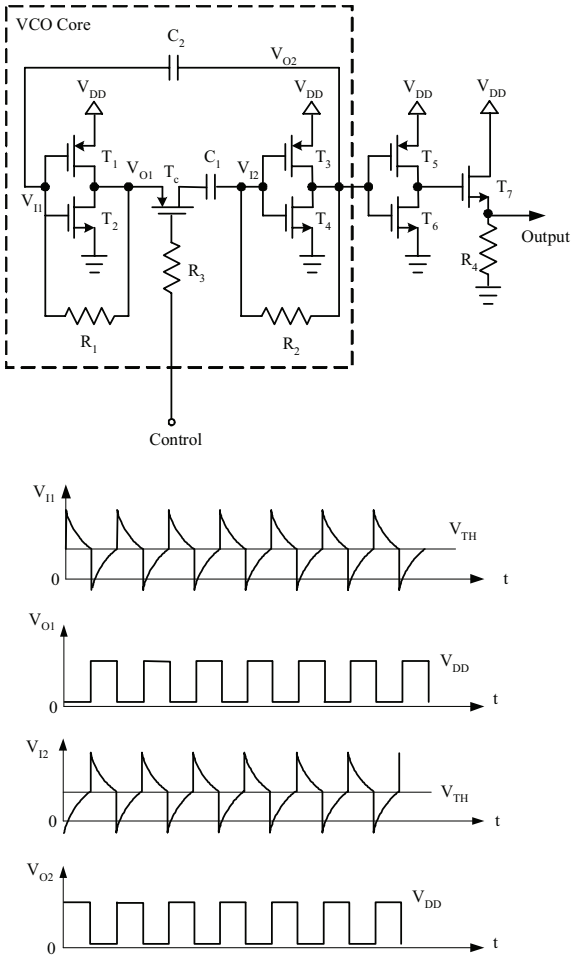

Figure 1. The proposed VCO diagram and its waveforms

relaxation oscillator [10]. In this oscillator, the transistors T_1, T_2, T_3 and T_4 compose two identical CMOS inverters, which can work as amplifiers with inversion if they are biased at the linear region. The proper biases for the two inverters are realized using two equal-value feedback resistors, R_1 and R_2. A positive-feedback loop is set up when these two properly-biased amplifiers are end-to-end connected via two capacitors, C_1 and C_2, as shown in Fig. 1. Self-oscillation can be built within this positive feedback loop. When the circuit is turned on and if there is any fluctuation to pull up the input of the first inverter, V_{I1}, it will induce a positive-feedback process in this loop as follows:

$$V_{I1} \uparrow \rightarrow V_{O1} \downarrow \rightarrow V_{I2} \downarrow \rightarrow V_{O2} \uparrow \rightarrow V_{I1} \uparrow$$

The positive feedback creates voltage jumps at the inputs of two inverters, as illustrated by the waveforms at the bottom of Fig. 1. Consequently, the output of the first inverter is "0" and the output of the second inverter (T_3 and T_4) is "1". This is the first state of the oscillator. At this time, the capacitors C_1 and C_2 begin to be charged and discharged through R_1 and R_2, respectively. V_{I2} is increased when C_1 is in charge. When V_{I2} goes over the input threshold voltage of the second inverter, the other positive-feedback process is induced:

$$V_{I2} \uparrow \rightarrow V_{O2} \downarrow \rightarrow V_{I1} \downarrow \rightarrow V_{O1} \uparrow \rightarrow V_{I2} \uparrow$$

This process results in the other state of the oscillator, "1" at the output of the first inverter and "0" at the output of the second inverter. The two capacitors C_1 and C_2 begin a reverse charge/discharge process compared to the first state, and will return the oscillator back to the first state when the two inverter inputs arrive at the threshold voltage of the inverters again. The oscillator core switches its output between these two states and its frequency is determined by the charge/discharge time of the capacitor C_1 or C_2.

The PMOSFET, T_C, with the resistor R_3 is introduced into the above symmetric relaxation oscillator in order to control the charge/discharge time, and thus achieve frequency control. The resistor R_3 here prevents the leakage of the VCO high-frequency signal to the external control voltage source. The output from the VCO core is then amplified by the buffer circuit, which includes a CMOS inverter and a voltage follower.

III. FREQUENCY CONTROL ANALYSIS

Fig. 2 gives charge/discharge models of the capacitor C_1. The capacitor C_2 has a similar operation as the capacitor C_1 due to the symmetric structure. The transistor T_C, controlled by its gate voltage, can be modeled as a tunable resistor R_C when it works in triode region [11]. The charge model shown in Fig. 2(a) corresponds to the first state aforementioned in Section II. The first inverter input V_{I1} is high and the second inverter input V_{I2} is low in this state. They turn on T_2 and T_3 respectively (with T_1 and T_4 turned off), so that the supply V_{DD} will charge the capacitor C_1 via the transistor T_3 (represented by $R_{ON(P)}$), the resistor R_2, the tunable resistor R_C and the transistor T_2 (represented by $R_{ON(N)}$), until the input of the second inverter V_{I2} arrives at its threshold, V_{TH}. The above charge time can be approximated as

$$T_{ch} \approx (R_{ON(P)} + R_2 + R_C + R_{ON(N)})C_1 \ln(\frac{V_{DD}}{V_{TH}}) \quad (1)$$

Fig. 2(b) illustrates the capacitor discharge model for the other state, where T_1 and T_4 are turned on, with T_2 and T_3 turned off. Due to the symmetric oscillator structure, the discharge time is equal to the charge time:

$$T_{disch} = T_{ch} \quad (2)$$

which is also illustrated by the waveforms in Fig. 1. A CMOS inverter usually has $V_{TH}=V_{DD}/2$, substituting this value into Eq. (1) and Eq. (2) yields,

$$T_{ch} = T_{disch} \approx 0.693(R_{ON(P)} + R_C + R_2 + R_{ON(N)})C_1 \quad (3)$$

A whole cycle of the charge/discharge process will be the sum of T_{ch} and T_{disch},

$$T = T_{ch} + T_{disch} = 1.38(R_{ON(P)} + R_C + R_2 + R_{ON(N)})C_1 \quad (4)$$

For $R_2 >> R_{ON(P)}$ and $R_2 >> R_{ON(N)}$, the above cycle time can be simplified as

$$T = 1.38(R_C + R_2)C_1 \quad (5)$$

Therefore, the VCO frequency only depends on R_C, R_2 and C_1 by

$$f = \frac{0.724}{(R_C + R_2)C_1} \tag{6}$$

It is clear from Eq. (6) that the proposed VCO's frequency can be adjusted by tuning R_C, the AC equivalent channel resistance of T_C. One way to calculate Rc is

$$R_c = \left(\frac{dI_{DS}}{dV_{DS}} \right)^{-1} \tag{7}$$

where V_{DS} is the drain-source voltage and I_{DS} is the drain current. I_{DS} here is given by the BSIM3 MOSFET SPICE model for submicron triode region [12]

$$I_{DS} = \mu_{eff} C_{ox} \frac{W(V_{GS} - V_T - A_{bulk} V_{DS} / 2)V_{DS}}{L + \frac{V_{DS}}{2E_{sat}}} \tag{8}$$

where μ_{eff} is the effective carrier mobility, C_{ox} is the oxide capacitance, W is the gate width, V_{GS} is the gate-source voltage, V_T is the threshold voltage, L is the gate length, E_{sat} is the saturated electrical field, and A_{bulk} is bulk charge effect and it is close to unity for small channel length [12].

IV. EXPERIMENTAL RESULTS

The proposed CMOS VCO was implemented using TSMC 0.18µm CMOS process. Fig. 3 shows a microphotograph of the fabricated VCO. The VCO circuit has a compact core size of just 80µm x 200µm (0.016 mm^2), or 560µm x 350µm including the pads. The gate width of transistor T_C was 120 µm. Resistors R_1 and R_2 were each 1 kΩ and C_1 and C_2 were each 0.6 pF. According to Eq. (6), the maximum frequency of this VCO was designed to be 1.2GHz (when $R_C = 0$).

The DC supply voltage was 1.8V in the measurements. The output frequencies versus the control voltage both from the circuit simulation and the measurement are shown in Fig. 4. Because of the parasitics in the fabricated VCO, it is noted that the measured frequency was lowered by about 50MHz compared to the frequency in the simulation. In the measurement, the free-running frequency of the VCO was 812 MHz and the frequency tuning was nearly linear from 650 MHz to 840 MHz with a control voltage from –1V to 0.4V, representing a tuning range of 28%. The maximum frequency of the VCO was 840MHz because of the non-zero turned-on channel resistance Rc. One way to reduce this resistance is to increase the DC supply, V_{DD}. According to Eq. (7) and Eq. (8), the change of V_{DD} affects the drain-source voltage V_{DS} of the transistor T_C, and therefore, reduces its triode resistance. The free-running frequency could reach beyond 1.1 GHz with a DC supply of 4.7V in the measurement, as close to the designed maximum frequency, 1.2GHz. Fig. 5 shows a sample of the frequency spectrum of the VCO at its free-running frequency, where the second and the third harmonics were 8 dB and 23 dB below the fundamental, respectively. Fig. 6 gives the output power measurement

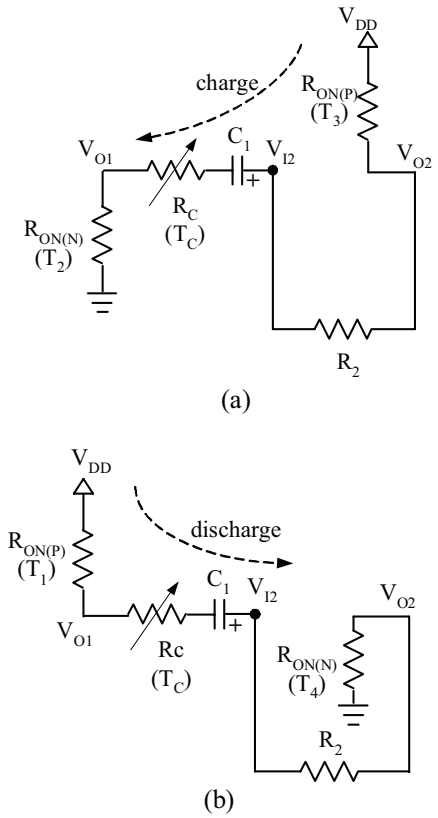

Figure 2. Capacitor charge/discharge models (a) charge-up (b) discharge

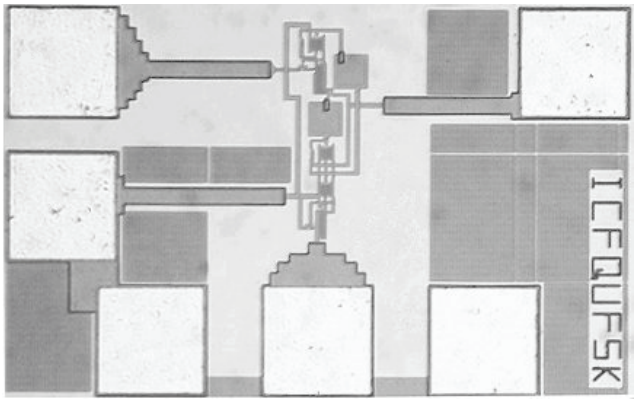

Figure 3. Microphotograph of the fabricated VCO

of the fabricated VCO at 1.8V DC supply. The output power was -14.5 dBm with only ±1 dB variation over the full frequency-tuning range. By changing the DC supply, the output power level was able to reach –6.5dBm at 4.7V DC supply. The DC power consumption was quite low for this VCO. It was measured to be only 5.4mW, or 3mA for the 1.8V DC supply.

Phase noise was also measured in order to investigate the noise performance of the VCO. Table 1 presents the measured phase noise values at 2 MHz and 10 MHz offsets at two different frequencies.

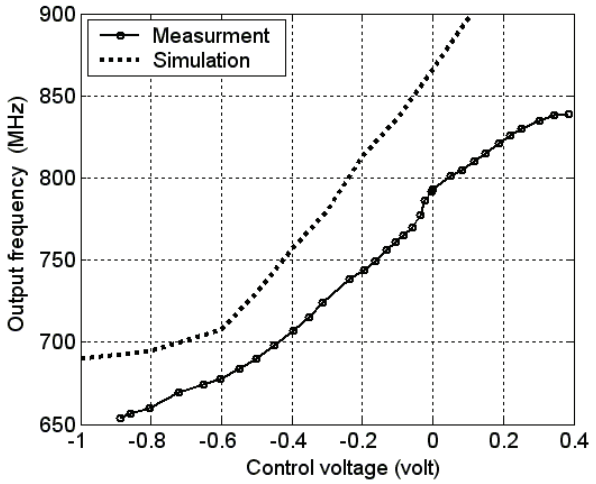

Figure 4. The output frequencies of the VCO versus its control voltage from the simulation and the measurement

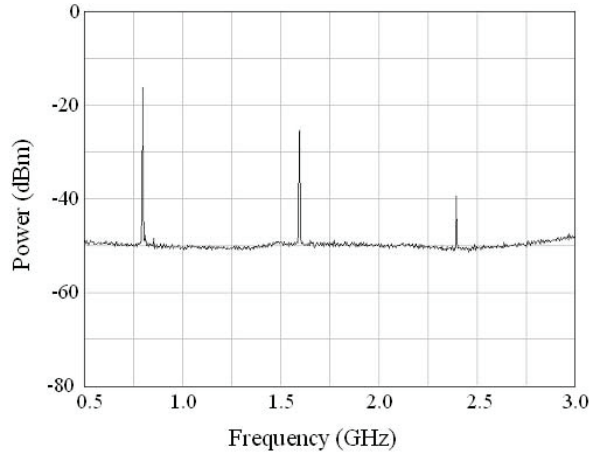

Figure 5. The VCO frequency spectrum

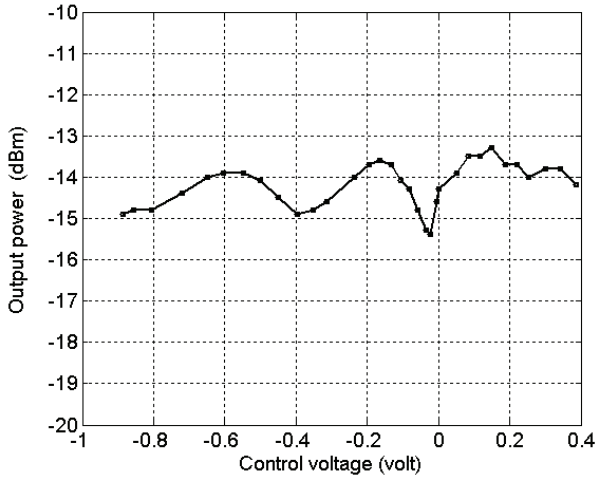

Figure 6. The output power of the fabricated VCO versus the control voltage

Table 1. Phase noise measurement

Frequency (MHz)	Phase Noise (dBc/Hz)	
	2MHz offset	10MHz offset
652	-66	-84.9
802	-64.6	-92

V. CONCLUSION

In this work, a single MOSFET was introduced for the frequency control of a relaxation oscillator, resulting in a compact CMOS relaxation-based VCO. The proposed method was demonstrated both in theoretic analysis and in the measurement of the fabricated VCO. The fabricated VCO circuit has a compact core size of only 0.016 mm^2 and a linear frequency tuning range from 650 MHz to 840 MHz. The output power was –14.5 dBm with only ±1 dB variation in the full tuning range and the corresponding DC power consumption was 5.4 mW. The frequency and the output power could be further increased beyond 1.1GHz and –6.5 dBm respectively, using higher DC voltage supply.

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