# Pulse Width Modulator Using a Phase-Locked Loop Variable Phase Shifter

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*Abstract*—**This paper presents a new concept for a pulse width modulator based on a voltage-variable phase shifter. A square waveform and a phase shifted version of itself is fed to a logic AND gate, which generates an output signal with 0 to 50 % duty cycle. By using a network of inverters after the AND gate, the duty cycle can reach up to 100 %. The phase shifter circuit is implemented using a novel phase-locked loop approach and it has a range of -180° to +180°.**

## I. Introduction

Pulse width modulation (PWM) is extensively used in electric motor speed control circuits, digital-to-analog conversion, and power supplies, to name but a few prominent applications. In PWM, the width of the pulses of a pulse train are proportional to the voltage level of the baseband information signal.

There exist several techniques for producing a width-modulated pulse train. Perhaps the most common method currently in use employs the comparator method in which a sawtooth waveform and the baseband signal are fed to a comparator and the output is a PWM waveform [1-5]. Recently, a pulse width modulator that does not use a comparator was proposed in [6]. In that work, two voltage-controlled delay lines are used in conjunction with an RS flip-flop to generate a 0-50% duty cycle at the output of the latch. To extend the duty cycle to 100%, two 0-50% modulators are used in parallel and combined.

In this paper, a new pulse width modulator concept is proposed which relies on a voltage-controlled phase shifter, a two-input logic AND gate, a network of logic inverters, and FET switches. The concept is to first generate a 0 to 50% pulse width using the phase shifter and an AND gate and then to extend the range to 0 – 100% using the inverters. The circuit easily lends itself to either discrete or monolithic implementation. One important advantage of this circuit is its potential for high carrier frequency operation. Whereas this PWM implementation shares in common the use of a delay (phase shift) with the modulator in [6], the two circuits differ significantly on how the 0 to 100% duty cycle is achieved. This paper is organized as follows: Section II details the design of the pulse width modulator. Section III is devoted to the variable phase shifter implementation, Section IV presents the experimental results, and Section V concludes the work.

## II. Modulator Concept

A pulse-width modulator having a 0 to 50 % duty cycle can be implemented by using feeding a square wave and a phase-shifted version of itself to a logic AND gate. The modulating signal is the input signal to the voltage-controlled phase shifter. If the phase shift between the input signals to the AND gate is 0°, then the output will have a 50% duty cycle. As the phase shift is increased, the duty cycle will decrease towards 0% as the phase shift reaches 180°. In the other direction, as the phase shift drops from 0° towards -180°, the duty cycle again decreases from 50% to 0%. It is clear, then, that additional circuitry is required to extend the duty cycle range from 50% to 100%.

To extend the duty cycle range, the solution is to invert the output signal of the AND gate when the phase shift drops below 0º. Consider the waveforms depicted in Figure 1a. At the top there is a phase shift, $\phi$, between the square wave signals $V_A$ and $V_B$. When these two signals enter the logic AND gate, the output signal, $V_g$, consists of a pulse train with a width W. Inverting $V_g$ leads to the signal at the bottom of Figure 1a which has a pulse width, T, that is between 50 % and 100 %. The schematic of the proposed 0 - 100% duty-cycle pulse width modulator is shown in Figure 1b.

In Figure 1b, the modulating wave $V_m$ tunes the phase shifter and thereby controls the pulse width at the output of the AND gate. In this discussion, the modulating voltage is assumed to be always positive and with a midpoint value of $V_{mid}$. For $V_m > V_{mid}$ the phase shifter produces a positive phase shift and conversely, for $V_m < V_{mid}$ the phase shift is negative. At the bottom of Figure 1b, the threshold of the Schmitt Trigger is set to $V_{mid.}$ When $V_m > V_{mid}$ the output of

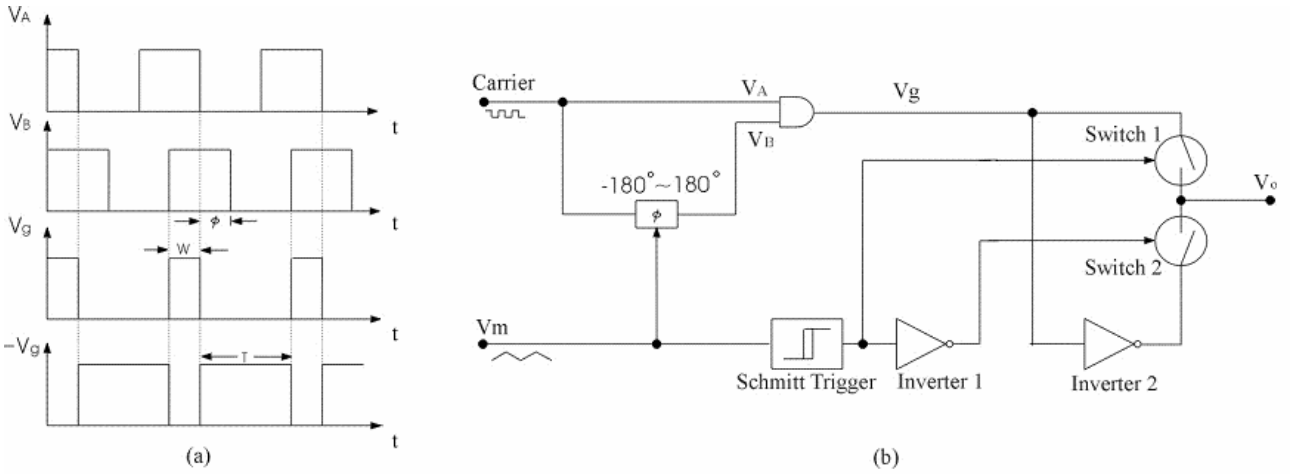


**Figure 1** a) Representative waveforms for duty cycles greater than 50 % b) proposed 0 to 100 % duty cycle pulse width modulator implementation.

the trigger will be 5 V and the voltage of the first inverter will be 0 V, which will activate FET Switch 1 and FET Switch 2 will be off and $V_g$ will pass through to the output, $V_o$. For $V_m < V_{mid}$ the output of the trigger will be 0 V and the output of Inverter 1 will be 5 V. As a result, Switch 1 will be off and Switch 2 will be activated. In this case, the inverted version of $V_g$ will pass through to $V_o$ (via inverter 2). In this manner the entire 0 to 100% duty cycle range is achieved.

## III. PLL Phase Shifter

Analog phase shifters can be implemented in a variety of ways. Some implementations use RC networks, vector summation [7,8], or frequency multiplication [9]. For digital signals, however, the choices are much more limited. In this work, we have used a novel phase-locked loop (PLL) approach because of its wide range and constant output amplitude performance. To date relatively few PLL-based phase shifters have been demonstrated; one previous implementation is described in [10].

A block diagram of the variable -180° to 180° phase shifter used in the modulator is shown in Figure 2a. The square-wave input signal, $V_{in}$, enters the phase shifter at the top phase detector ($PD_1$) and the phase-shifted signal is taken at the output of the voltage controlled oscillator (VCO). The PLL is composed of $PD_1$, the top low pass filter ($LPF_1$), a summing junction, and the VCO. $V_f$ is simply an offset voltage to set the central frequency of the VCO. Assume for simplicity that initially the voltages V- and $V_+$ into the summing junction are equal to zero. In this case, the VCO will be locked to the input signal and therefore the phases of the input and output signals will be 180° out-of-phase due to the presence of inverter 2. Note that, $V_{d1}$ and $V_+$ will be equal to zero.

Inverter 1 produces a 180° phase shift on the output signal, $V_o$, which is then fed to the second phase detector ($PD_2$) in conjunction with $V_o$ itself. Due to the constant 180° phase shift between the inputs to $PD_2$, the output signal after the second low-pass filter ($LPF_2$) will be a constant regardless of the phase difference between $V_{in}$ and $V_o$. Following $LPF_2$ there is a potentiometer which ultimately controls the phase shift between $V_{in}$ and $V_o$. If the potentiometer is set to 0 Ω then the signal V- into the summing junction will be zero and the phase shift between $V_{in}$ and $V_o$ will be 180°. As the resistance $R_{k2}$ is increased, there will be a non-zero voltage, V-, into the summing junction. Since the input signal to the VCO has to be zero when the PLL is in lock, the voltage $V_+$ at the output of $LPF_1$ must be equal to V-. In order to generate this non-zero voltage, $V_+$, the phase difference between $V_{in}$ and $V_o$ must now be such that $PD_1$ generates a constant non-zero output voltage. In this manner, a sustained phase shift between $V_{in}$ and $V_o$ is achieved.

Without the amplifier in the second feedback loop, the range of this phase shifter would be only 0° to 180° because the maximum voltage of V- would be equal to $V_{d2}$ (see Figure 2a). By incorporating the amplifier, V- can be increased beyond $V_{d2}$ and thus the phase shift range can be extended to the full 360°. Referring to Figure 2a, the output phase of the VCO is given by,

$$\theta_o = \frac{K_o K_{d1} F_1(s)}{s}(\theta_{in} - \theta_o) + \frac{K_o K_{d2} F_2(s)}{s}(K_r \times G \times 180^\circ) \quad (1)$$

where $K_o$ is the VCO gain constant, $K_{d1}$ and $K_{d2}$ are the phase detector constants, $F_1(s)$ and $F_2(s)$ are the transfer functions of the first and second low-pass filters respectively, $\theta_{in}$ is the input phase angle, $K_r$ is the potentiometer resistance ratio, and G is the gain of the amplifier. The phase shift can be written as,

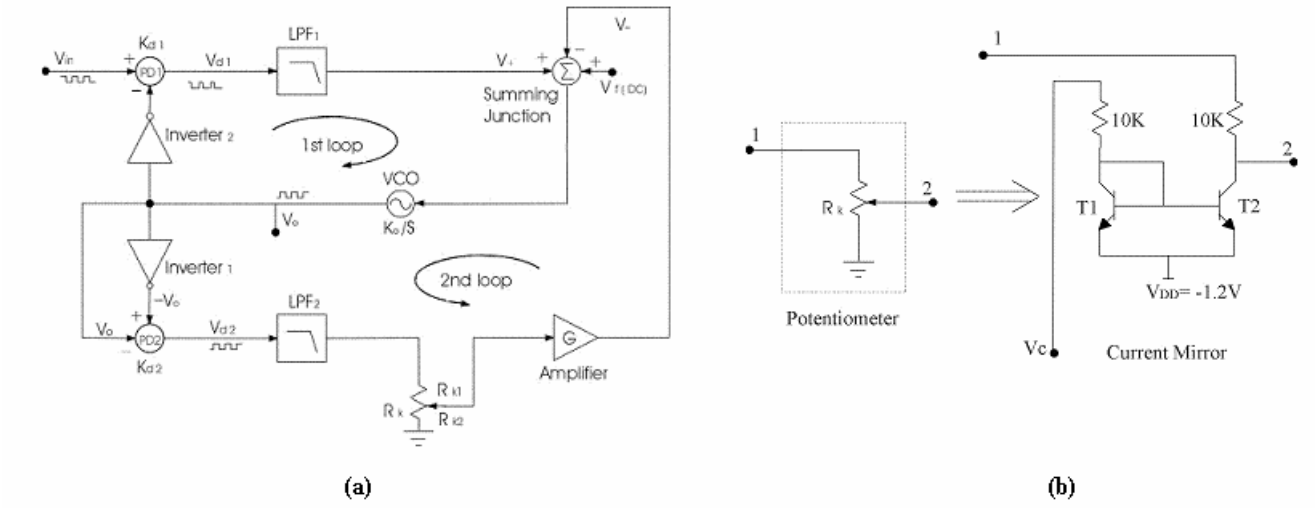


**Figure 2** a) Phase-locked loop variable phase shifter b) electronic control implementation.

$$\theta_e = \theta_{in} - \theta_o$$
$$= \frac{s}{K_o K_{d1} F_1(s) + s}\theta_{in} + \frac{K_o K_{d2} F_2(s)}{K_o K_{d1} F_1(s) + s}(K_r \times G \times 180^\circ) \quad (2)$$

Arbitrarily setting $\theta_{in}$ equal to zero, equation (2) can be simplified to,

$$\theta_e = \frac{K_o K_{d2} F_2(s)}{K_o K_{d1} F_1(s) + s}(K_r \times G \times 180^\circ) \quad (3)$$

which explains the importance of the amplifier gain, G. In this expression, the fraction term is less than 1 and can be regarded as a loss. Since $K_r = R_{k2}/R_k$ is used to change the phase shift, it is also less than or equal to 1. As discussed previously, the maximum phase shift $\theta_e$ would be less than 180º if the gain element, G, is absent.

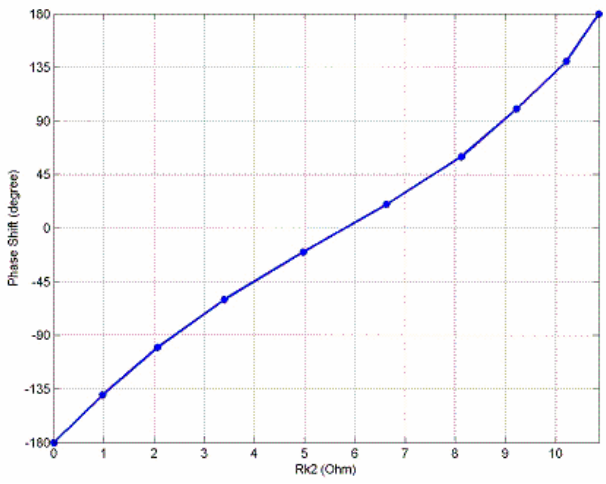


**Figure 3 -** Phase-locked loop phase shifter response.

In the circuit of Figure 2a, a potentiometer is used to vary the phase shift. This was done to help explain the behavior of the circuit. In practice, one needs electronic phase-shift control and to that end, the circuit in Figure 2b was used instead of the potentiometer. This circuit is, in effect, a voltage-controlled voltage source with $V_m$ (the baseband signal) being the control voltage, $V_c$. Figure 3 depicts the measured phase response of the PLL phase shifter from -180° to 180°.

## IV. PWM Experimental Results

The pulse width modulator depicted in Figure 1b was built using packaged components. Packaged digital PLLs with 1-pole RC low-pass filters ($f_{cutoff}$=850Hz) were used for the phase shifter. The Schmitt Trigger was implemented using a high-speed operational amplifier. The slew-rate of the operational amplifier was 45V/μs and its unity-gain bandwidth was 20 MHz. In this modulator, the Schmitt trigger is the frequency-limiting component. For high-speed operation, a monolithic trigger implementation using CMOS devices can significantly improve performance.

The rise time of the CMOS inverters was 30 ns, which is a negligible fraction (< 0.05%) of the period of the 11 kHz pulse train used for the carrier. Thus, the delay introduced by the inverters did not affect the pulse width of the output waveform. Lastly, Switches 1 and 2 were realized using two n-channel MOSFET transistors with a threshold voltage of about 2.1 V.

The bottom trace in Figure 4 shows the output of the pulse-width modulator in the time domain. The top trace is a triangular modulating signal ($V_m$) with a peak-to-peak voltage of 2 Volts and a frequency of 500 Hz. Modulating frequencies of up to 5 kHz were used, and much higher carrier frequencies are possible by correspondingly increasing the cut-off frequency of the low-pass filters and the frequency of the VCO in the PLL phase shifter.

The pulse width of the output signal versus the modulating voltage, $V_m$, is depicted in Figure 5. It is seen in this figure that the pulse width varies nearly linearly (within experimental error) over the entire range from 0 % to 100 %. The small deviation of the measured curve from the ideal straight line was determined to come from the PLL phase shifter response.

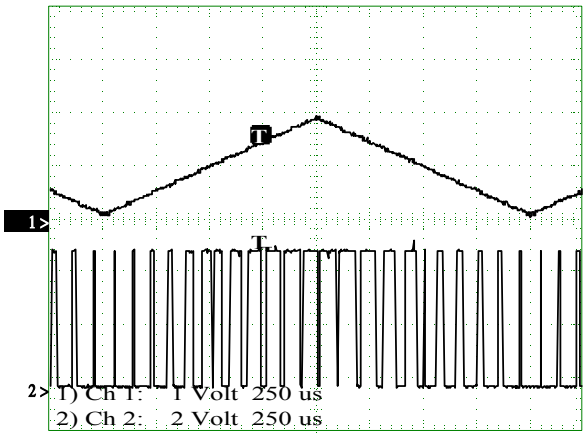


**Figure 4** - Pulse width modulator input and output signals

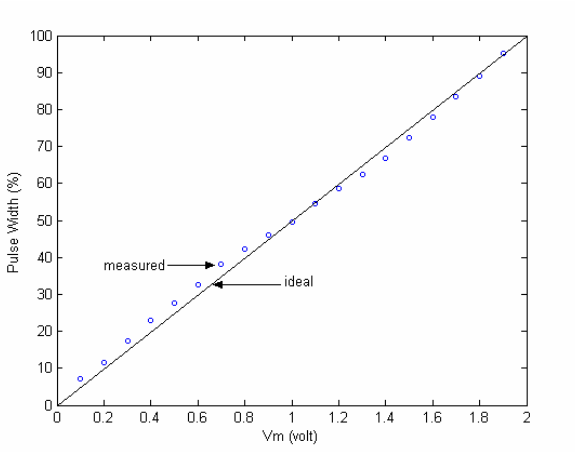


**Figure 5** - Output pulse width (duty cycle) versus input control voltage

## V. Conclusion

A new concept for a pulse width modulator based on a variable phase shifter has been demonstrated in this work. The most critical part of this modulator is the phase-shifter, which must be capable of producing a linear phase shift versus control voltage over a 360º span. The experimental results confirm the feasibility of this pulse-width modulator.

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