A BPSK Demodulator Circuit using an Anti-Parallel Synchronization Loop

You Zheng and Carlos E. Saavedra
Department of Electrical and Computer Engineering
Queen's University
Kingston, Canada
2yz2@qlink.queensu.ca

***Abstract*—A novel anti-parallel loop carrier synchronization method for BPSK demodulation is proposed and demonstrated in this work. The method contains an anti-parallel dual loop, which locks the carrier by its upper loop and lower loop alternately, according to the data bits contained in the received BPSK signal. Simulation and experimental results are shown along with BER performance.**

I. INTRODUCTION

Satellite communications have unique advantages over other types of communications, such as large coverage over geographical areas and capability of broadcasts directly to the public and end-to-end connections directly to users. Currently, several satellite systems use Binary Phase Shift Keying (BPSK) modulation. One the most well-known systems using BPSK is the INMARSAT satellite network, which is used primarily by ocean-going vessels. Another important satellite network using BPSK modulation is the Global Positioning System (GPS). To reduce the cost of a satellite receiver it is essential that new methods for the demodulation of BPSK signals be found which can reduce the size and the complexity of the overall system.

To demodulate BPSK, circuits such as the squaring loop [1][2], the remodulator loop [3], and the Costas loop [4] are widely used. The PLL-based demodulators are all coherent detectors. There also exist 'non-coherent' BPSK demodulators that use pulse detection by differentiating the incoming modulated signal [5], and others that use encoding at the source such as in the Differential BPSK (DBPSK) case, and that only require a delay element and a mixer at the receiver [1].

An anti-parallel carrier synchronization method for BPSK demodulation is proposed in this work, resulting in a new BPSK demodulator. This method has a simple structure and contains easily-integrated elements, and thus is competitive with the Costas loop. In the section II, the proposed method is described with its operation and mathematical analysis. The demonstration of the proposed method with simulation and experimental results is presented in Section III, and Section IV concludes this work.

II. CIRCUIT OPERATION

The proposed carrier synchronization method is shown in Figure 1. It contains a dual loop with a 180° phase shifter in the lower loop, so-called anti-parallel loop here. The phase detectors used for this anti-parallel loop utilize two multiplier-type detectors, plus a DC offset V_{dc} at each detector. The DC offsets are introduced using two voltage summers and they play important role for the operation of this anti-parallel loop. Moreover, there are two switches at the VCO input and a control circuit: a comparator and an inverter.

The concept here is that with proper control of the switches, an anti-parallel dual loop with 180° phase difference can offer the locking to a received BPSK signal, which switches its phase between 0° and 180° in accordance with the data. For example, when the received BPSK signal is at 0° phase, the upper switch closes and the lower switch opens, and therefore the output of the upper loop is fed to the VCO and it operates like a single PLL (the upper loop works as demodulation loop in this case); When the received BPSK signal switches its phase to 180°, the upper switch opens and the lower switch closes, and thus the lower loop will operate as the locking loop.

Proper control of the switches is required for the above operation. The control circuit of the switches requires a voltage difference between its two inputs in order to produce the control signal. If the two DC offsets were removed from Fig. 1 and the upper loop locked first, the upper detector output would be zero (assuming the input carrier frequency was equal to the centre frequency of the VCO). The phase difference between its two inputs is -90° at this time,

0-7803-8834-8/05/$20.00 ©2005 IEEE.

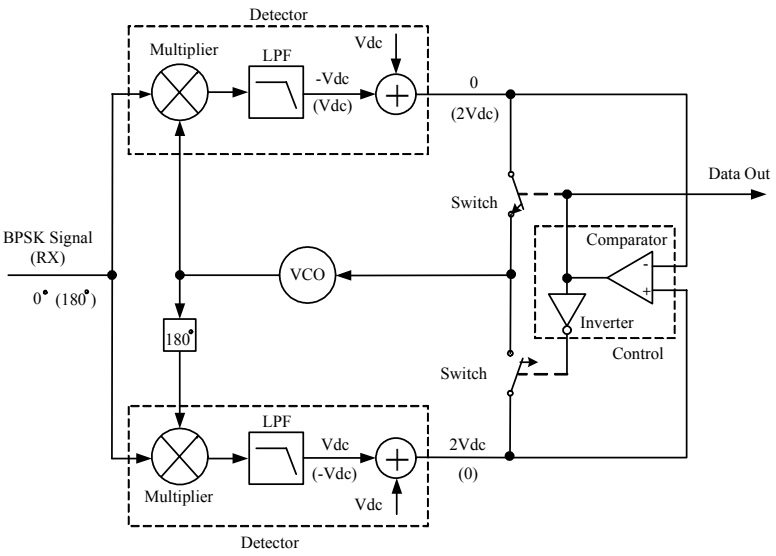


Figure 1. Circuit diagram of the proposed BPSK demodulator

according to the characteristic of the multiplier-type detector. At the same time, due to the 180° phase shifter at the lower loop, the input phase difference for the lower detector was 90°, which results in a zero output at the lower detector, too. Because the inputs of the control circuit come from these two detector outputs, the control circuit cannot properly distinguish these two zero inputs, and would fail to give the proper control signal for the switches.

With the DC offsets introduced, the multiplier-type detectors can produce the different outputs in this anti-parallel loop and meet the above requirement. In Fig. 1, if the upper loop locks first, the VCO's phase is driven to let the upper detector output a zero voltage. A $-V_{dc}$ voltage is produced from the upper multiplier-type detector in order to cancel the DC offset V_{dc} at the output of the upper voltage summer. At the same time, the voltage from the lower multiplier-type detector is $+V_{dc}$, which is the inverse of that of the upper multiplier-type detector due to the 180° phase difference between the two loops. As a result, the output of the lower detector will be $2V_{dc}$. Thus, this $2V_{dc}$ voltage output at the lower loop and the zero output at the upper loop are fed to the comparator in the control circuit together to produce a high-voltage signal to close the upper switch (the inverter produces a lower-voltage signal to open the lower switch). These switch states are exactly what we need. When the phase of the received BPSK signal switches 180°, the lower detector outputs zero instead and the upper detector outputs $2V_{dc}$. The control signal after the comparator is inverted and turn on the lower switch only, then the lower detector's output (zero) is fed to the VCO to lock its phase.

The input of the VCO above keeps at zero whenever the received BPSK signal switches its phase in accordance with the data. Therefore, the data information contained in the BPSK signal is removed by switching the locking loop between the two loops, and then the carrier is recovered. It can be noted that the control signal from the comparator switches between high-voltage and low-voltage in accordance with the phase of the received BPSK signal. It is exactly the demodulated data signal. Thus, a coherent BPSK demodulator is realized based on this anti-parallel method illustrated in Fig. 1.

The following mathematical analysis of the proposed demodulator gives more operation details for the proposed demodulator. Assume that the received BPSK signal has the form

$$S(t) = A_1 \cos(\omega_c t + \theta_1 + \varphi) \tag{1}$$

where θ_1 represents the received carrier phase, and φ bears the data information and switches between 0° and 180°. This received signal is multiplied by $A_2\cos(\omega_c t+\theta_2)$ and $-A_2\cos(\omega_c t+\theta_2)$, which are the outputs from the VCO and the 180° phase shifter, respectively. The two multiplier-type detector outputs after the low-pass filters (the high frequency products of the multipliers are removed by the low-pass filters) are

$$U(t) = k_d \cos(\theta_e + \varphi) \tag{2}$$

$$L(t) = -k_d \cos(\theta_e + \varphi) \tag{3}$$

where $k_d = (A_1A_2/2)$ is the phase detector gain and $\theta_e=\theta_1-\theta_2$ is the initial phase difference between the carrier and the VCO. The multipliers are assumed to have a unit gain to simplify the analysis. Note that these two outputs are inversed with each other, which explains the inversion of the outputs between the upper and the lower multiplier-type detectors in the previous description. After summed with the DC offsets V_{dc} at the voltage summers, the final detector outputs are

$$U'(t) = k_d \cos(\theta_e + \varphi) + V_{dc} = \pm k_d \cos(\theta_e) + V_{dc} \tag{4}$$

$$L'(t) = -k_d \cos(\theta_e + \varphi) + V_{dc} = \mp k_d \cos(\theta_e) + V_{dc} \tag{5}$$

where the data information φ alternates between 0° and 180°, resulting in a "±" sign for the cosine functions. As we can see, the two outputs in the equations (4) and (5) alternates oppositely between two voltage values

$$V_1 = k_d \cos(\theta_e) + V_{dc} \quad \text{and} \quad V_2 = -k_d \cos(\theta_e) + V_{dc} \qquad (6)$$

Since the configuration of the control circuit in the anti-parallel loop only allows the detector output with smaller value to pass the switches and enter the VCO, if the initial value of $\cos(\theta_e)$ before locking is negative, the first value V_1 in the equation (6) is the smaller one and it is selected as the error voltage to drive the VCO, regardless of which loop it is from. Thus, the data information φ or the "±" sign in the equations (4) and (5) is eliminated by the control from the control circuit. When the VCO is locked, its input error voltage V_1=0 volt, which results in

$$k_d \cos(\theta_e) = -V_{dc} \qquad (7)$$

Substituting the above value to the expression in the equation (6) yields the other detector output

$$V_2 = -k_d \cos(\theta_e) + V_{dc} = V_{dc} + V_{dc} = 2V_{dc} \qquad (8)$$

The V_1 (i.e. zero) and V_2 (i.e. $2V_{dc}$) are then fed to comparator to produce the data output and the proper control signal as well.

In the above analysis, the VCO is locked to the upper loop first as the result of $\cos(\theta_e)<0$. However, if the initial value of $\cos(\theta_e)$ before locking is positive, the locking state in the above case will be reversed, i.e. V_2 is the smaller one and is chosen for the error voltage to drive the VCO. When the VCO is locked, V_2=0 volt and $V_1=2V_{dc}$. In this case, the comparator outputs a low voltage in order to turn on the lower switch only, which results in an inversion on the data output compared to the last case. This data inversion phenomenon exists at other coherent demodulators too and can be further solved by differential coding/decoding technique [6].

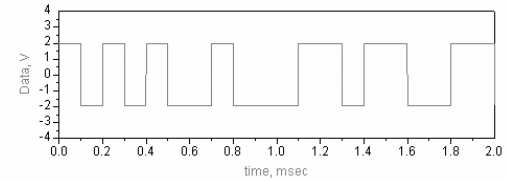
The DC offsets determine the detector outputs in the proposed demodulator, and they cannot exceed the maximal output of the multiplier-type detector, k_d, according the equations (4), (5) and (6). The proposed demodulator still works if there is difference between these two DC offsets. In this case, the detector of the demodulation loop will output $(V_{dc1}+V_{dc2})$ instead of $2V_{dc}$, where V_{dc1} and V_{dc2} represents the two different DC offsets. The detector output of the locking loop still keeps zero in this case. For the case that there was a small deviation on the carrier frequency of the input BPSK signal, the two detectors will output a small voltage of δ and $(2V_{dc}-\delta)$ instead of zero and $2V_{dc}$ respectively, when the loop is locked. Note that the two detectors still have different outputs to ensure the demodulator operation till δ exceeds V_{dc}. Other mismatches between the two loops, such as the detector-gain mismatch and the loop-filter mismatch, could come from circuit implementation. The detector-gain mismatch has similar effect as the DC-offset mismatch described above. The loop-filter mismatch causes different locking speeds between the two loops, and the highest data rate is mainly determined by the lower-speed loop.

The proposed demodulator is similar to the Costas loop, but gets rid of the third multiplier used in the Costas loop, which, usually realized on Gilbert cell in IC implementation, would double the number of the loop filters, because Gilbert cell requires differential inputs. Moreover, the used 180º phase shifter is more easily-integrated than the 90º phase shifter. The switches can be realized on two N-MOSFETs, which was demonstrated in the experiment as described below. The DC offsets can utilize DC bias in the multipliers.

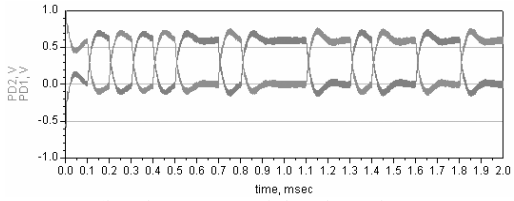
III. Simulation and Experimental Results

The proposed BPSK demodulator was simulated using the simulator Advanced Design System (ADS) from Agilent Technologies. For demonstration purposes, the center frequency of the VCO was set to 133 kHz. A pseudo random bit sequence (PRBS) data with a rate of 10 kbps was used in this simulation, which is slightly higher than the data rate 9.6kbps used in INMARSAT systems [7]. Two RC LPFs with cutoff frequency of 14.4kHz were used for the loop filters in the phase detectors. The detector gain and the gain constant of VCO were optimized to achieve a damping factor of 0.7 for the PLL [8]. The detector gain was 1volt/rad and the DC offsets were set to 0.3 volt.

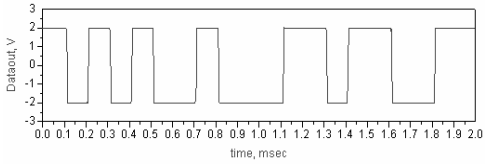
Fig. 2 shows the data contained in the received BPSK signal, the detector outputs and the successfully-demodulated data from the simulation, respectively. The initial phase difference between the carrier and the VCO was 220º for this simulation, resulting in a negative value for $\cos(\theta_e)$, thus there was no inversion on the demodulated data according to



(a) The PRBS data for the modulation

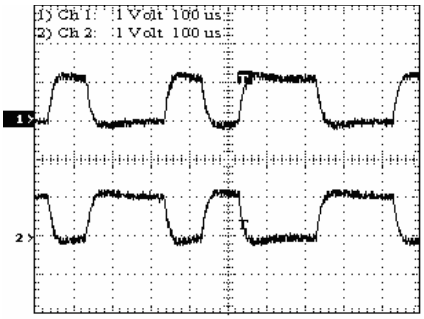


(b) The outputs of the phase detectors (after the voltage summers)

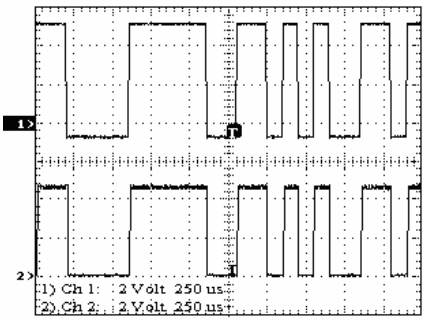


(c) The demodulated PRBS data (after the comparator)

Figure 2. The simulation results for θ_e = 220°



(a) The outputs of the detectors for V_{dc}=0.5V (after the two amplifiers)



(b) The PRBS data for modulation (Channel 1) and the demodulated data (Channel 2)

Figure 3. The captured waveforms in the experiment

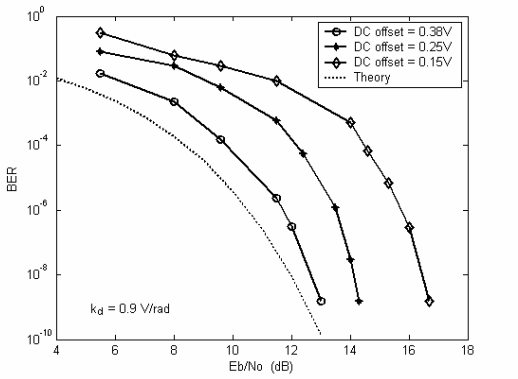


Figure 4. BER versus E_b/N_0 on different DC offset values.

the analysis in the previous section. The detector outputs alternated between 0 volt and 0.6 volt, i.e. $2V_{dc}$, as predicted in the previous description. Other simulations with different values of $\cos(\theta_e)$ were also carried out and the results were consistent to the analysis of this demodulator.

Based on the above simulations, a test circuit was built using packaged integrated circuit components. Two four-quadrant analog multipliers were chosen for the phase detectors, which had an additional summing input and was utilized for the DC offsets needed in this demodulator. The VCO and LPFs had same parameters as in the simulation. An amplifier with a gain of -1 was used for the 180° phase shifter. The switches were implemented using two N-MOSFETs with symmetric configuration. The detector gain was 0.9 volt/rad and the damping factor of the loops was also optimized to 0.7 in the experiment.

The BPSK signal generator used for the test was implemented using a multiplier circuit to multiply a carrier signal with a PRBS NRZ data coming from an HP 3764A Digital Transmission Analyzer (DTA). The NRZ data from the DTA was transformed to be symmetric data (±2 volt) before it went into the multiplier. Fig. 3 presents the experimental waveforms captured from a test with a DC offset of 0.5 volt. Fig. 3(a) gives the outputs of the two detectors. Note that the two outputs offset with each other and their voltage levels were 0 volt and $2V_{dc}$=1 volt, which were exactly expected according the analysis. Fig. 3(b) gives the PRBS data (Channel 1) used for test and the successfully-demodulated data (Channel 2) from the BPSK demodulator. It needs to be pointed out that the two figures shown in Fig. 3 were captured at different times and thus contained different data information (the PRBS data varies with time). The case that the demodulated data would contain an inversion of the modulating PRBS data was also observed sometimes when the circuit was reset in the experiments. Fig. 4 shows the measured bit error rate (BER) versus bit energy to noise density (E_b/N_0) in several DC offset values, as well as an ideal curve for the BPSK demodulator from theory. The measured BER curve got close to the ideal curve when the DC offset went up. It indicated that BER performance can be improved by use of as large DC offset as allowed in the proposed demodulator.

IV. CONCLUSION

An anti-parallel synchronization method for BPSK demodulation has been demonstrated both in simulation and experiment. Due to its simple structure and easily-implemented elements, this demodulator is competitive with other BPSK demodulation techniques such as the Costas Loop or the remodulator loop.

REFERENCES

[1] Lawrence E. Larson, *RF and Microwave Circuit Design for Wireless Communications*, Artech House, Boston, London, 1997.

[2] L. E. Franks,"Carrier and bit synchronization in data Communication-a tutorial review," *IEEE Trans. on Comm*., vol.COM-28, pp.1107-1121, August 1980

[3] T. Shimamura,"On False-Lock Phenomena in Carrier Tracking Loops," *IEEE Trans. on Comm*.,vol.28, pp.1326-1334, Aug. 1980.

[4] J. Costas, "Synchronous Communications," *IEEE Trans. on Comm.*, vol.5, pp. 99-105, Mar. 1957.

[5] A. Tan and C. E. Saavedra, "A Binary Phase Shift Keying Demodulator using Pulse Detection," *IEEE Int. Conference on Electrical and Electronics Engineering,* pp. 49-52, 2004.

[6] R. E. Ziemer and R.L. Peterson, *Digital Communication and Spread Spectrum Systems*, MacMillan Publishing Company, New York, 1985.

[7] INMARSAT LTD., Maritime Communications and Safety, http://maritime.inmarsat.com/

[8] Roland E. Best, *Phase-Locked Loops, Design, Simulation, and Applications*, McGraw-Hill, Toronto, 2003.