AN M-PSK MODULATOR FOR QUASI-OPTICAL WIRELESS ARRAY APPLICATIONS

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ABSTRACT

A new phase shift keying modulator particularly suited for quasi-optical oscillator-array applications is described. Experimental results for a 28 GHz BPSK version of the general M-PSK modulator are presented.

INTRODUCTION

For efficient spectrum utilization, linear digital modulation schemes such as Quadrature Amplitude Modulation and Phase Shift Keying (PSK) are widely used [1]. Arrays of oscillators can be modulated by injection locking the elements to an external source which itself is modulated. However, this requires a high-frequency feed from the external reference into the array. Alternatively, a phase-locked loop (PLL) can be used to lock a voltage-controlled oscillator array so that only a low frequency connection is required [2]. Conventional PLL's are restricted to phase shifts of less than $\pm 90°$ and so are unsuitable for PSK modulators where larger phase swings are required. The modulator described here overcomes this limitation with a unique dual PLL loop to key a VCO over the complete phase space (Figure 1).

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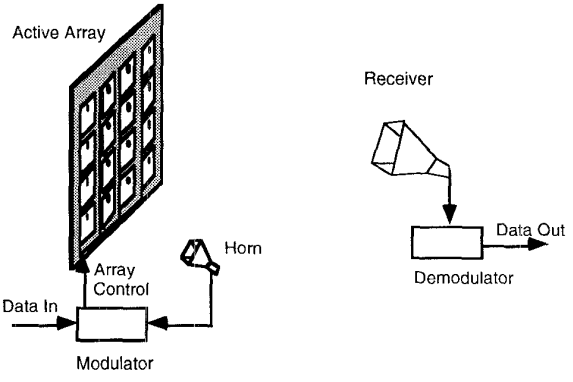

Figure 1 Wireless quasi-optical link in which modulation is achieved using an external modulator. The oscillator array is controlled by a feedback loop in which a portion of the array's output is compared with a reference signal.

MODULATOR DESIGN

A schematic of the modulator is shown in Fig. 2. Output from the oscillator feeds two mixers that are driven by a low phase-noise reference carrier. Output from the mixers are multiplied by In-phase (I) and Quadrature (Q) message signals, $m_1(t)$ and $m_2(t)$. The outputs are summed, filtered, and fed to the oscillator bias or to varactor tuning elements.

Ignoring the double-frequency components from the mixers, the input to the filter can be written as,

$$V_c(t) = K_d K_m[\sin(\theta_i - \theta_0)m_1(t) + \cos(\theta_i - \theta_0)m_2(t)]$$

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where θ_i and θ_0 are the phases of the reference and VCO signals. K_d and K_m represent the responses of the reference and modulation mixers, respectively. V_c can be rewritten in the form,

$$V_c(t) = K_{de} \sin(\theta_i + \theta_m - \theta_0) \tag{1}$$

where $m_1(t) = A\cos\theta_m(t)$, $m_2(t) = A\sin\theta_m(t)$, and $K_{de} = K_d K_m A$.

the phase θ_m ramps between two values θ_{m1} and θ_{m2} in time ΔT, then the phase error, or loop stress is given by [3]

$$\theta_e = \frac{\theta_{m2} - \theta_{m1}}{\Delta T K_0 K_{de} F(0)} \tag{2}$$

where K_0 is the VCO constant. To keep this error small, the dc filter response, $F(0)$, must be made large, at the expense of increasing the loop instability and noise-bandwidth.

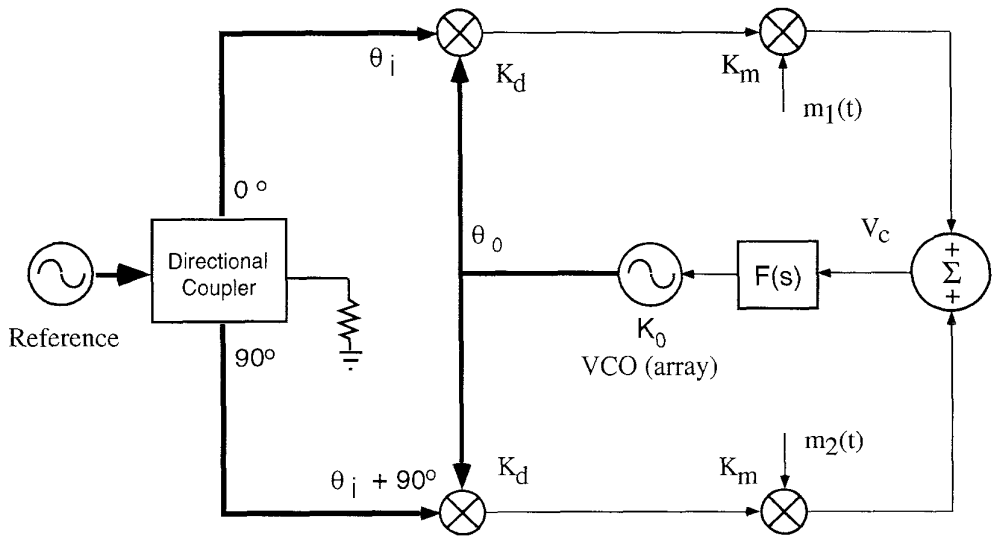

Figure 2 M-PSK Modulator schematic. The thick lines represent the high-frequency interconnects, and the thin lines indicate the baseband connections.

Equation (1) indicates that the modulator can be represented as a single PLL in which the equivalent phase of the reference, $\theta_i + \theta_m$, is a function of the two message signals, $m_1(t)$ and $m_2(t)$. In steady-state operation the array locks to the reference with a phase offset of θ_m. If $m_1(t)$ is constant and $m_2(t)$ is a square-wave with zero DC component, then the modulation is binary-PSK. Quadrature-PSK modulation is obtained by using square wave for both message signals. In a similar manner, 8-PSK is achieved with $[m_1(t), m_2(t)]$ alternating between the relative levels $[\frac{-1}{\sqrt{2}}, \frac{-1}{\sqrt{2}}]$, $[-1, 0]$, $[\frac{-1}{\sqrt{2}}, \frac{1}{\sqrt{2}}]$, $[0, -1]$, $[0, 1]$, $[\frac{1}{\sqrt{2}}, \frac{-1}{\sqrt{2}}]$, $[1, 0]$, and $[\frac{1}{\sqrt{2}}, \frac{1}{\sqrt{2}}]$. If $m_1(t), m_2(t)$ are chosen so that

NUMERICAL SIMULATIONS

Transient behavior of the modulator of Figure 2 was examined in the time domain using the Omnisys simulator in the HP-HFDS software package. The transmitted and received baseband signals for a 28 GHz carrier and 500 Mbps data rate are shown in Fig. 3.

With each change in input state, the loop overshoots then settles into the desired state. This appears as crosstalk between the quadrature and in-phase channels, as evidenced by the spikes in the received data signals in figure 3 at times $t = 2$ nsec, and $t = 10$ nsec.

The overshoot and settling time can be controlled by appropriate choice of filter, $F(s)$, in a manner analogous to single loop design [3,4]. When the loop is in lock $V_c(t)$ is very small, hence the summer inputs (Fig. 2) are approximately equal in magnitude but opposite in sign. If the signs of both message signals change simultaneously, the summer inputs will remain opposite in sign and $V_c(t)$ will momentarily remain zero until the loop reacts. Hence, there is a time delay before the loop tracks the phase shift at times $t = 6$ nsec and $t = 8$ nsec (Fig. 3).

In practice, this delay can be virtually eliminated by varying $m_1(t)$ and $m_2(t)$ so that the equivalent phase θ_m varies uniformly and K_{de} is constant. At times $t = 2$ nsec and $t = 10$ nsec the loop reacts instantaneously because only one of the signal inputs is changing, so that $V_c(t)$ will be non-zero at the signal transition.

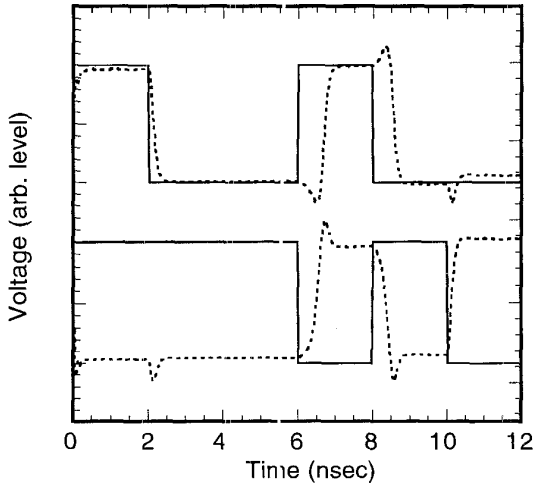

Figure 3 Simulated transient behavior for the QPSK modulator. The solid lines are the input message waveforms for the I and Q carriers, and the dashed lines are the recovered signals.

EXPERIMENTAL VERIFICATION

A binary phase shift keying (BPSK) version of the M-PSK modulator was built and tested at 28 GHz. For BPSK modulation, only the one half of the circuit is used. An HP 8350B sweep oscillator with $K_0 = 123 \times 10^6$ rad/V, served as the VCO element. A 20 GHz source was used to mix down the 28 GHz VCO signal to lock to an 8 GHz reference signal from an HP 83622A synthesizer. A Watkins-Johnson MY50 mixer was used for the high-frequency down-conversion, and a WJ-18C mixer was used as a phase detector. For the modulation multiplier in the baseband part of the circuit, an Analog Devices AD 834JN multiplier was used. A lag-lead network was used as the loop filter, with the pole at 0.65 MHz, and the zero at 6.25 MHz. The DC gain of the loop was carefully adjusted until lock was achieved. The baseband electronics (multipliers, op amps) add additional poles and zeros to the loop transfer function. If the DC gain of the system is sufficiently large, pole(s) appear in the right-half of the $s-$plane and the loop will be unstable [3].

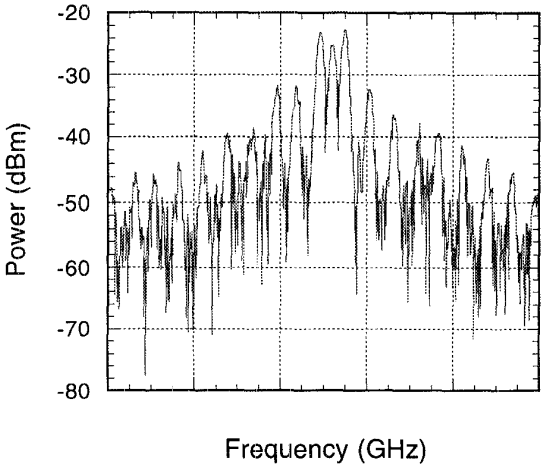

Figure 4 Measured carrier spectrum. The center frequency is 28.3719 GHz and the bandwidth is 50 kHz.

The plot in figure 4 shows the spectrum of the modulated signal. The modulation corresponds to a data rate of 3.2 kbps. This data rate is limited by poles in the baseband electronics.

CONCLUSIONS

The M-PSK modulator presented here is well suited for quasi-optical arrays because the modulation circuitry is at baseband, thereby reducing the complexity and cost of achieving phase modulation with the arrays. Furthermore, multichannel transmission is possible by using a separate modulator for each array element. A prototype BPSK modulator has been built and tested at Ka Band.

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REFERENCES

[1] L. J. Greenstein and M. Shafi, *Microwave Digital Radio*, New York: IEEE Press, 1988.

[2] M. J. Vaughan and R. C. Compton, "Phase Noise in Arrays of Mutually-Coupled Oscillators and its Reduction via Injection-Locking and PLLs," submitted to *IEEE Trans. Microwave Theory Tech.*, Oct. 1995.

[3] F. M. Gardner, *Phaselock Techniques*, New York: John Wiley & Sons, 1979.

[4] S. M. Shinners, *Modern Control System Theory and Design*, New York: John Wiley & Sons, 1992.