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A 5-GHz energy-efficient tunable pulse generator for ultra-wideband applications using a variable attenuator for pulse shaping

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SUMMARY

A new energy-efficient tunable pulse generator is presented in this paper using 0.13-μm CMOS technology for short-range high-data-rate 3.1–10.6 GHz ultra-wideband applications. A ring oscillator consisting of current-starved CMOS inverters is quickly switched on and off for the duration of the pulse, and the amplitude envelope is shaped with a variable passive CMOS attenuator. The variable passive attenuator is controlled using an impulse that is created by a low-power glitch generator (CMOS NOR gate). The glitch generator combines the falling edge of the clock and its delayed inverse, allowing the duration of the impulse to be changed over a wide range (500–900 ps) by varying the delay between the edges. The pulses generated with this technique can provide a sharp frequency roll off with high out-of-band rejection to help meet the Federal Communications Commission mask. The entire circuit operates in switched mode with a low average power consumption of less than 3.8 mW at 910 MHz pulse repetition frequency or below 4.2 pJ of energy per pulse. It occupies a total area of $725 \times 600\,\mu m^2$ including bonding pads and decoupling capacitors, and the active circuit area is only $360 \times 200\,\mu m^2$. Copyright © 2011 John Wiley & Sons, Ltd.

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KEY WORDS: ultra-wideband; pulse generator; CMOS integrated circuits; Radio Frequency (RF) analog circuits; impulse radio

1. INTRODUCTION

Ultra-wideband (UWB) systems, which are regulated by the Federal Communications Commission (FCC) for commercial use in the 3.1- to 10.6-GHz frequency band, are promising for short-range wireless data communication, imaging, and high-precision ranging applications. Impulse UWB technology using short duration impulses has drawn much attention from researchers and industry as it potentially offers several advantages, including high data rates, low power and complexity, reduced multipath fading, high time and range resolution, and low probability of undesired detection and interception. Energy-efficient and low-cost impulse UWB transceivers [1, 2] are attractive for wireless communication and biomedical applications such as wireless personal area networks [3–9], interchip communications [10–13], and UWB biotelemetry [14–16]. Sub-nanosecond pulse generation is a critical function in pulsed UWB transceivers, posing some serious challenges in circuit design. In addition to the wide bandwidth required, low power and low complexity (for low cost) are necessary. A pulse generator should also be tunable for different pulse shapes and spectra to handle process variations, regulatory differences, and changes in the channel or antenna characteristics.

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Traditional UWB pulse generators have used some specific components such as step recovery diodes [17–20], which are difficult to integrate in standard CMOS and suffer from limited tunability. Other pulse generators form an impulse at baseband and then upconvert it to the target frequency band as in narrow-band carrier-based systems [21–24]. These tend to be quite complex and power hungry because of the use of continuously running local oscillators and/or mixers. Switched or gated local oscillators have been investigated to reduce circuit complexity and power consumption [25–27]. However, the oscillator turn-on and stabilization time can be relatively long, limiting the energy efficiency, pulse width, and pulse repetition frequency (PRF). In addition, there is little control over the start-up and turn-off transients, and the output pulse shape cannot be readily tuned. Direct (carrier-less) UWB pulse generators have also been demonstrated using exponential and/or differentiating circuits and filters [3, 7, 9–15, 28, 29]. They typically use large passive devices and/or provide only one specific pulse shape that cannot be tuned. Furthermore, fast digital-to-analog converters have been used for direct UWB waveform synthesis and can provide high resolution and tunability [30, 31]. However, high sampling and data rates are typically required (e.g., 20 and 120 Gb/s, respectively [30]), which results in high power and circuit complexity. Finally, distributed waveform generators have been reported using digital delay lines, edge combiners, and/or transmission lines [4, 6, 8, 16, 32–34]. Nevertheless, their distributed nature typically leads to a large area and power consumption.

In this paper, a new energy-efficient tunable pulse generator is presented in 0.13-μm CMOS for short-range high-data-rate 3.1- to 10.6-GHz UWB applications. A ring oscillator consisting of current-starved CMOS inverters is quickly switched on and off over the duration of the pulse, and the output amplitude is shaped using a variable passive attenuator. The variable passive attenuator consumes zero DC power and has a wide bandwidth. It is controlled using an impulse, which is created by a low-power glitch generator (CMOS NOR gate). The glitch generator combines the falling edge of the clock signal and its delayed inverse to form the impulse. This allows the duration of the pulse to be changed over a wide range (500–900 ps) by simply varying the delay between the edges. The generated pulses can provide a sharp frequency roll off with high out-of-band rejection, which is beneficial in satisfying the FCC spectrum limits. The entire circuit operates in switched mode with zero static current for a low average power consumption of less than 3.8 mW at 910 MHz PRF or below 4.2 pJ of energy per pulse. It occupies a total area of $725 \times 600\,\mu m^2$ including bonding pads and decoupling capacitors, and the active circuit area is only $360 \times 200\,\mu m^2$.

2. CIRCUIT ARCHITECTURE AND DESIGN

A block diagram of the UWB pulse generator is shown in Figure 1(a). It mainly consists of a current-starved ring oscillator, a glitch generator, and a variable attenuator. An inverter chain first sharpens the rising/falling edge of the clock signal, which is used to turn the ring oscillator on and off. The clock signal is then split into two branches in the glitch generator, one of which is delayed and inverted with respect to the other. A NOR gate combines the falling and rising edges of these signals to form an impulse, whose duration can be tuned over a wide range by varying the delay between the edges. This impulse controls the variable attenuator to shape the amplitude envelope of the ring oscillator's signal and form the desired UWB pulse at the output. Note that the pulse generator can support on–off keying modulation and pulse position modulation by directly modulating the input clock signal with the baseband digital data. Figure 1(b) shows the complete circuit schematic.

2.1. Current-starved ring oscillator

The ring oscillator [2, 11, 12, 22, 35, 36] has a very short start-up time because of its low quality factor, which is important for low-power high-data-rate UWB applications. However, the oscillation frequency can be limited by power consumption and CMOS technology. In this work, three current-starved CMOS inverters are cascaded in a ring or loop as shown in Figure 1 to

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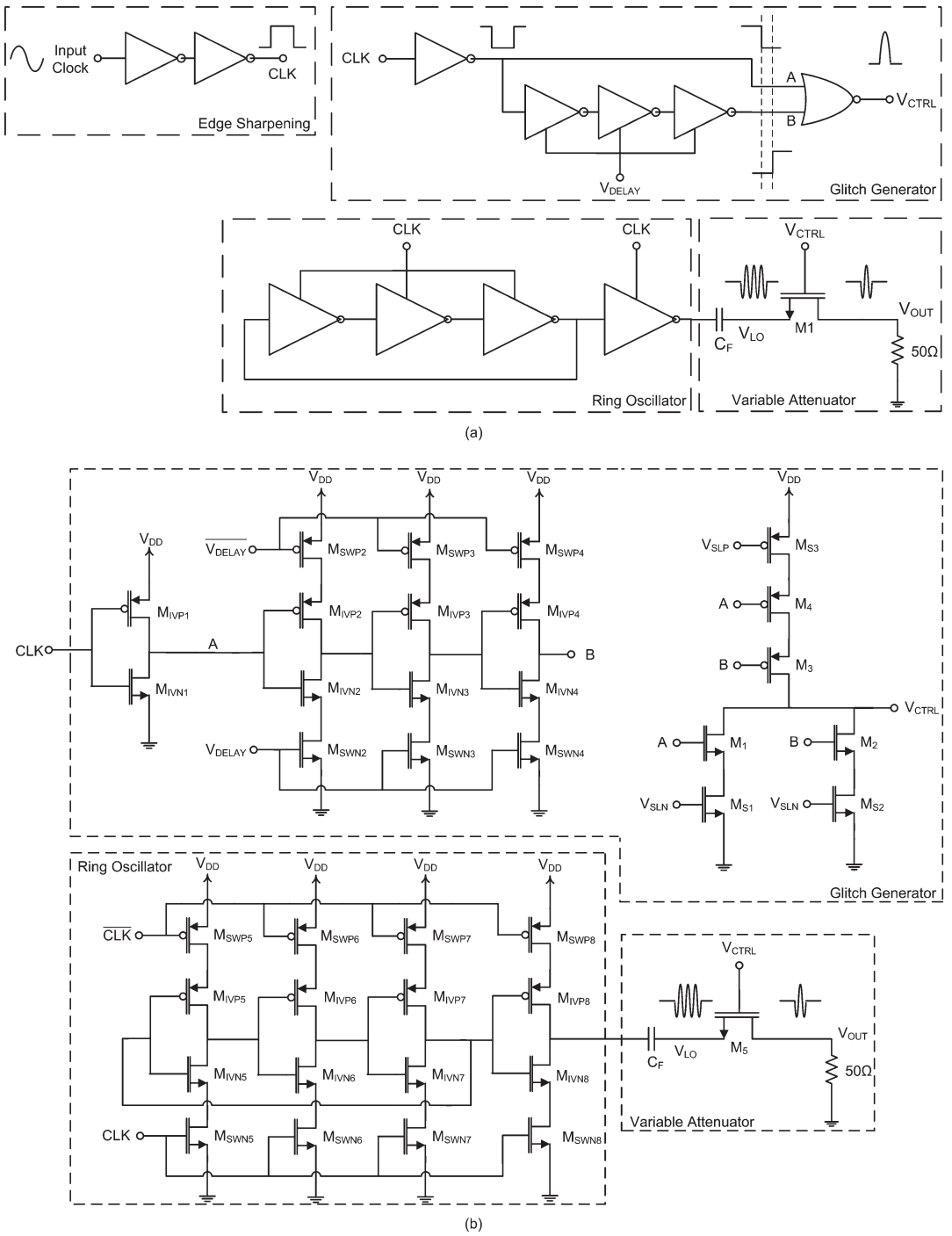

Figure 1. Proposed UWB pulse generator: (a) block diagram and (b) circuit schematic.

produce an oscillating waveform with a fixed frequency when the series NMOS and PMOS devices (M_{SWN} and M_{SWP} in Figure 1(b)) are switched on by the clock signals. To compensate for the lower mobility of holes and generate a symmetric waveform with equal rise and fall times, PMOS devices (M_{IVP} and M_{SWP}) are made larger than NMOS devices (M_{IVN} and M_{SWN}) such that their effective on-resistance is approximately equal to that of the NMOS devices. The equivalent on-resistance of the NMOS and PMOS devices (R_{eqn} and R_{eqp}) is given by [37]:

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$$R_{\text{eqn}} \propto \frac{1}{I_{\text{dsatn}}}, R_{\text{eqp}} \propto \frac{1}{I_{\text{dsatp}}}, \tag{1}$$

where

$$I_{\text{dsatn}} = \frac{\mu_{\text{n}} C_{\text{oxn}}}{2} \frac{W_{\text{n}}}{L} (V_{\text{dd}} - V_{\text{tn}})^2 \frac{1}{1 + \frac{(V_{\text{dd}} - V_{\text{tn}})}{LE_{\text{satn}}}}, \tag{2a}$$

$$I_{\text{dsatp}} = \frac{\mu_p C_{\text{oxp}}}{2} \frac{W_p}{L} \left(V_{\text{dd}} - |V_{\text{tp}}|\right)^2 \frac{1}{1 + \frac{\left(V_{\text{dd}} - |V_{\text{tp}}|\right)}{LE_{\text{satp}}}}. \tag{2b}$$

I_{dsatn} and I_{dsatp} are the drain currents through the NMOS and PMOS devices, respectively, under velocity saturation. μ_n and μ_p are the electron and hole mobilities, C_{oxn} and C_{oxp} are the gate oxide capacitances per unit area, W_n and W_p are the device widths, L is the gate length, E_{satn} and E_{satp} are the saturation electric fields, and V_{tn} and V_{tp} are the threshold voltages. For the 0.13-μm CMOS technology used, $\mu_{\text{n}}=5.27\times10^{-2}\text{m}^2\text{V/s}$, $\mu_{\text{p}}=0.89\times10^{-2}\text{m}^2\text{V/s}$, $C_{\text{oxn}}=1.16\times10^{-2}\text{F/m}^2$, $C_{\text{oxp}}=1.08\times10^{-2}\text{F/m}^2$, $L=120\text{nm}$, $E_{\text{satn}}=3.27\times10^{6}\text{V/m}$, $E_{\text{satp}}=1.39\times10^{7}\text{V/m}$, $V_{\text{tn}}=0.43\text{V}$, and $V_{\text{tp}}=-0.43\text{V}$. Therefore, from Equation (2), the saturation drain current through the NMOS and PMOS devices (I_{dsatn} and I_{dsatp}) are approximately equal if

$$W_{\text{p}} = 3.12W_{\text{n}} \approx 3W_{\text{n}}, \tag{3}$$

at which point,

$$R_{\text{eqn}} \approx R_{\text{eqp}}. \tag{4}$$

The oscillation time T and frequency f are set by the propagation delay t_{p} through an inverter: $T=2Nt_{\text{p}}=6t_{\text{p}}$, $f=1/T=1/6t_{\text{p}}$. The inverter delay can be minimized by careful design to maximize the oscillation frequency without consuming excessive power. The series connection of the switching and inverter devices (M_{SW} and M_{IV} in Figure 1(b)) can be viewed as a distributed resistor–capacitor (RC) network, consisting of the transistors' equivalent on-resistance (R_{sw} and R_{iv}) and the internal and output node capacitances (C_{int} and C_{out}), as illustrated in Figure 2. It is important to note that the NMOS and PMOS device widths are ratioed

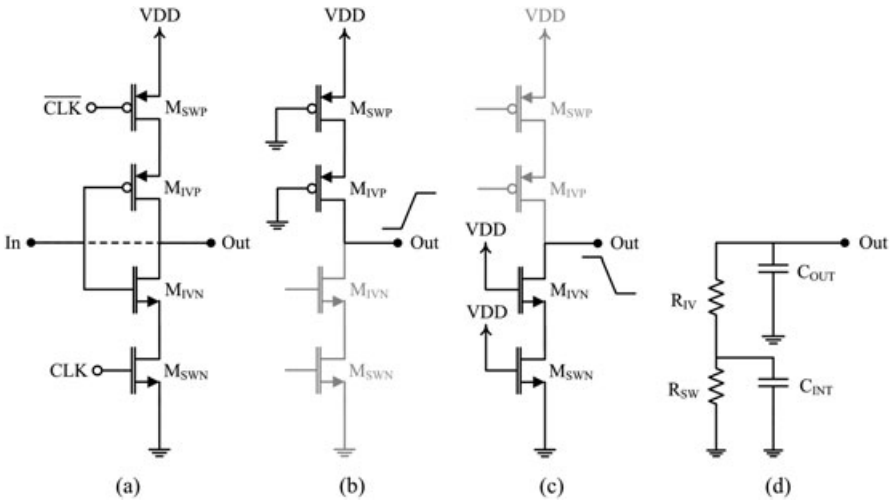

Figure 2. Current-starved inverter cell: (a) inverter schematic, (b) state in the low-to-high transition, (c) state in the high-to-low transition, and (d) equivalent resistor–capacitor network.

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(W_{swp}=3W_{swn}, W_{ivp}=3W_{ivn}) for equal on-resistance to yield a symmetric output waveform with equal rise and fall times. The RC network shown in Figure 2 can be used to represent the NMOS half and the PMOS half of the inverter during the high-to-low and low-to-high output transition, respectively. The time constant τ associated with the output transitions can also be approximated as follows [38]:

$$\tau \approx R_{sw}C_{int} + R_{sw}C_{out} + R_{iv}C_{out} \tag{5}$$

Because the on-resistance (R_{sw}) of the switching device and the output capacitance (C_{out}) each appear in two of the terms and thus dominate the delay, the width of the switching device should be made as large as possible (limited by power constraints), whereas that of the inverter device should be made relatively small for an oscillation frequency in the 5-GHz range.

A more detailed analysis of the ring oscillator was performed to arrive at the optimum inverter device sizes that lead to the maximum oscillation frequency for the chosen switching device sizes of W_{swn}=24μm and W_{swp}=72μm. Two of the small-signal models shown in Figure 3(a) are used to represent each inverter, one for the NMOS half and another for the PMOS half. The models include the parasitic capacitances (C_{gsiv}, C_{gdiv}, C_{dbiv}, C_{sbiv}, C_{gdsw}, C_{dbsw}), transconductance (g_{miv}), and output resistances (R_{oiv}, R_{osw}) of the devices. The parasitics and transconductance are calculated by assuming that the inverter and switching devices are operating in velocity saturation and triode, respectively. The *Y*-parameters (Y_{11}, Y_{12}, Y_{21}, Y_{22}) shown in Figure 3(b) for the small-signal model are given by

$$Y_{11} = \frac{Y_{gs}(Y_{ds} + Y_s)}{Y_s + Y_{gs} + G_m + Y_{ds}} + Y_{gd} \tag{6a}$$

$$Y_{12} = \frac{-Y_{gs}Y_{ds}}{Y_s + Y_{gs} + G_m + Y_{ds}} - Y_{gd} \tag{6b}$$

$$Y_{21} = \frac{G_m Y_s - Y_{gs}Y_{ds}}{Y_s + Y_{gs} + G_m + Y_{ds}} - Y_{gd} \tag{6c}$$

$$Y_{22} = Y_{db} + \frac{Y_{ds}(Y_{gs} + Y_s)}{Y_s + Y_{gs} + G_m + Y_{ds}} + Y_{gd} \tag{6d}$$

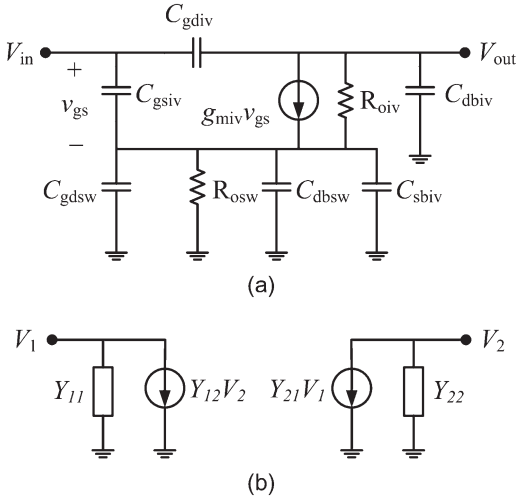

Figure 3. Inverter cell modeling and analysis: (a) small-signal model for the PMOS or NMOS half with parasitic capacitances and output resistances, and (b) equivalent *Y*-parameter network.

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and the admittances (Y_s, Y_{gs}, Y_{gd}, Y_{ds}, Y_{db}) and transconductance G_m are

$$Y_s = \frac{1}{R_{osw}} + j\omega\left(C_{gdsw} + C_{dbsw} + C_{sbiv}\right) \tag{7a}$$

$$Y_{gs} = j\omega C_{gsiv}, \quad Y_{gd} = j\omega C_{gdiv} \tag{7b}$$

$$Y_{ds} = \frac{1}{R_{oiv}}, \quad Y_{db} = j\omega C_{dbiv} \tag{7c}$$

$$G_m = g_{miv} = \frac{\mu C_{ox}}{2}\frac{W}{L}[V_{ov}||LE_{sat}]\frac{V_{ov} + 2LE_{sat}}{V_{ov} + LE_{sat}} \tag{7d}$$

where the overdrive voltage V_{ov} is $V_m - V_t$. V_m is the switching threshold of the inverter, which is approximately $V_{dd}/2$, because the PMOS and NMOS device widths are ratioed ($W_{swp}=3W_{swn}$, $W_{ivp}=3W_{ivn}$) for asymmetrical voltage transfer characteristic.

The equivalent *Y*-parameter model for the inverter can be calculated by adding the *Y*-parameters computed for the NMOS and PMOS circuits, because they are connected in parallel between the input and output nodes. The complete ring oscillator can then be analyzed by cascading three of these *Y*-parameter models in a positive feedback loop as shown in Figure 4. Performing Kirchhoff's Current Law (KCL) at nodes V_2 and V_3 and solving for the voltage gain per stage ($A_v=V_2/V_1$, etc) gives

$$A_v = \frac{Y_{12}^2 - Y_{21}(Y_{22} + Y_{11})}{(Y_{22} + Y_{11})^2 - Y_{12}Y_{21}} \tag{8}$$

The zero-loop-phase condition of the Barkhausen's criterion for oscillation can thus be met if

$$\angle A_v = \angle\left[\frac{Y_{12}^2 - Y_{21}(Y_{22} + Y_{11})}{(Y_{22} + Y_{11})^2 - Y_{12}Y_{21}}\right] = 120^\circ \tag{9}$$

Equation (9) yields a relationship between the oscillation frequency (ω) and the inverter device width (W_{ivn}). Figure 5(a) shows a plot of the oscillation frequency versus the inverter device width (W_{ivn}) that satisfies Equation (6c). Theoretically, the maximum (unloaded) oscillation frequency of the oscillator is 5.94 GHz when the inverter device width is 6.5 μm as observed in Figure 5(b). Using a wider device does not increase the oscillation frequency and only consumes more power. In simulation, the optimum inverter device size was ultimately found to be slightly below 6.5 at 5 μm.

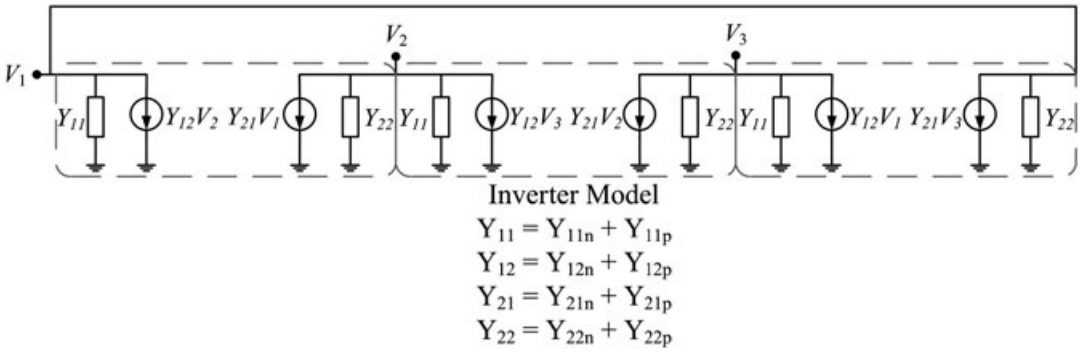

Figure 4. Ring oscillator model with three inverter *Y*-parameter models and positive feedback.

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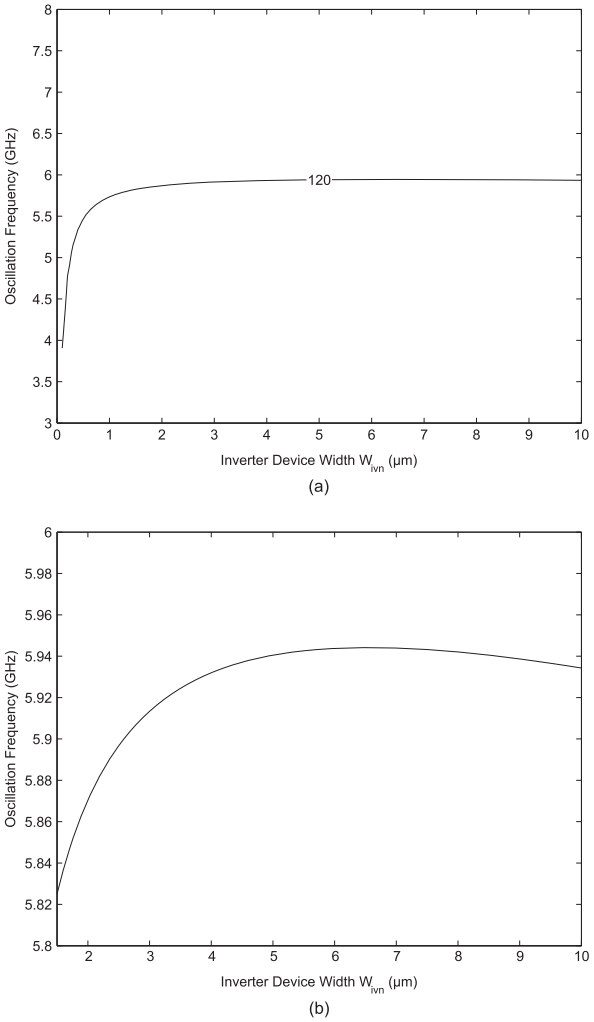

Figure 5. Ring oscillator frequency variation with inverter device width W_{ivn} for chosen switching device width of W_{swn}=24 μm: (a) plot of 120° phase contour and (b) plot of 120° contour more closely shown to depict the optimum device width for the maximum oscillation frequency.

This minimizes the delay to less than 28.5 ps for a maximum (unloaded) oscillation frequency of 5.88 GHz. Note that this analysis and optimization of the inverter device width was repeated for a range of switching device sizes. Using a switching device width smaller than W_{swn}=24 μm can only generate a lower oscillation frequency, whereas using a larger device width can generate the desired oscillation frequency but at the cost of increased power consumption.

2.2. *Glitch generator*

The sub-nanosecond glitch generator [39–42] shown in Figure 1 is an important component in creating the wideband signal having the required duration and shape. The pulse produced must be sharp and narrow enough (sub-nanosecond duration) to ensure high bandwidth. At the same time, it should be tunable to allow for longer durations and lower bandwidths. The main block in the glitch generator is the CMOS NOR gate shown in Figure 1(b). The output of this gate is high only if both inputs are low. An impulse can be created in a glitch fashion by feeding the gate with a clock falling edge along with its delayed inverse (*A* and *B* in Figure 1). The short duration where both signals are low causes the NOR gate's output (V_{CTRL}) to be temporarily pulled high, thus generating the pulse (Figure 1). This period also specifies the duration of the pulse. The delayed, inverted signal is realized using three cascaded current-starved CMOS inverters similar to those in the ring oscillator, as shown in Figure 1.

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This allows for the delay and thus the pulse duration to be varied by changing the gate voltage of the series devices. In addition, series devices are also added to the NOR gate (M_{S1}, M_{S2}, and M_{S3} in Figure 1(b)) to control the (dis)charging current and thus tune the rise/fall times (slopes) of the output pulse for a high out-of-band rejection.

The performance of the NOR gate can be optimized to maximize the pulse bandwidth. The PMOS (M_{S3}, M_{S4}, and M_{S3}) and NMOS (M_1, M_2, M_3, and M_{S2}) devices are sized such that the pull-up and pull-down equivalent pathresistances are roughly equal for a symmetric output pulse with equal rise and fall times. Furthermore, the pull-up (M_3, M_4, and M_3) and pull-down (M_1, M_2, M_{S1}, and M_{S2}) series devices are progressively sized to minimize the RC time constants (Equation (5)) and maximize the pulse bandwidth. The performance of the NOR gate also depends on input ordering. The critical input signal, that is, the last signal that undergoes a transition and switches the output, should be connected to the transistor closest to the output of the gate. The delayed rising edge (B) that signals the end of the pulse is the most critical and is thus connected to the PMOS device M_3 at the output. As soon as the rising edge arrives, M_3 turns off and the pull-down NMOS devices M_1, M_2, M_{S1}, and M_{S2} need to discharge only the output (V_{CTRL}) node capacitance. This speeds up the high-to-low transition of the output pulse for faster operation. Otherwise M_3 would remain on and both output and internal node capacitances would need to be discharged, slowing down the transition.

The optimum size for each device is determined by extensive simulation. Figure 6 is a comparison between the generated impulse in simulation and the Gaussian pulse given by

$$p(t) = A_p e^{-\left(\frac{t}{\tau}\right)^2} \tag{10}$$

where A_p is the pulse amplitude, which is the supply voltage V_{dd}=1.2V in this case, and τ=155*ps* is the pulse width and shape parameter. The shape of the generated impulse is close to that of the Gaussian pulse with a mean squared error of only 1.3% relative to the mean square value of the Gaussian pulse, and the duration of the impulse is about 400ps. Figure 7 shows the simulated glitch generator output as the impulse duration and shape are tuned. It is clear that the pulse can have a duration ranging from about 350 ps to about 800 ps. The pulse peak voltage also remains roughly constant at the supply voltage of V_{dd}=1.2V for all pulse durations.

2.3. Variable attenuator

A variable passive attenuator is used for pulse shaping as opposed to a variable gain amplifier, for instance, because the attenuator consumes zero DC power and has a small footprint, which is particularly useful in low-power, low-cost UWB applications. It also has a wider bandwidth and higher dynamic range with comparable devices. This comes at the cost of insertion loss.

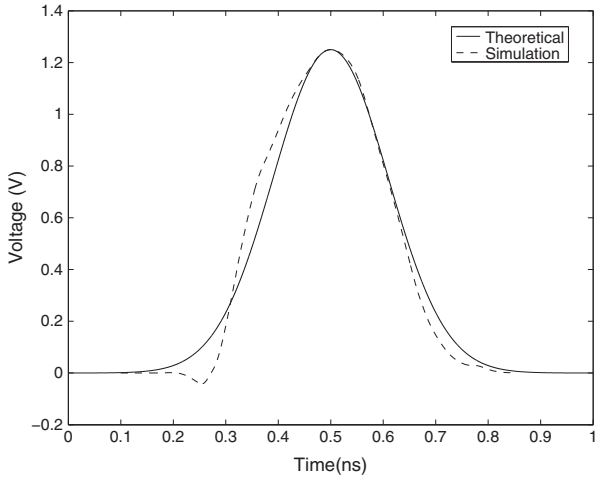

Figure 6. Generated baseband impulse and the Gaussian pulse with an amplitude of 1.2V and time duration of 400ps.

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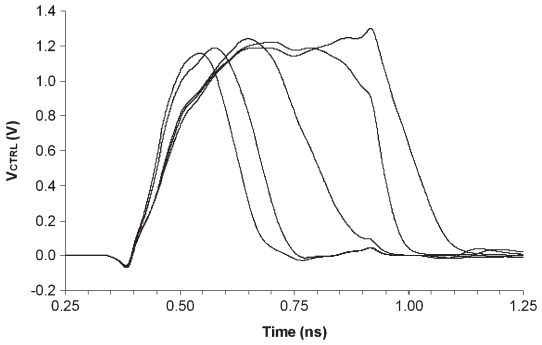

Figure 7. Simulated impulses with varying durations.

A variable resistor-based attenuator can be readily implemented on-chip by using a zero-biased MOSFET, with the resistance and attenuation controlled by the gate voltage. The bandwidth of the attenuator is thus inherently limited by the parasitic capacitances of the MOSFET. To reduce the parasitic capacitance for higher bandwidth, a single series NMOS device M_5 is used as shown in Figure 1(b). The conventional π-network has a higher attenuation range, but two inverted impulse signals are needed to control the series and shunt devices, and the higher parasitic capacitance can diminish the gain in attenuation range at higher frequencies. Furthermore, because the oscillator is switched off after pulse transmission, the required attenuation range forthe attenuator is relaxed. As shown in Figure 1(b), M_5 is driven by the pulse V_{CTRL} produced by the glitch generator. When the impulse voltage level is low (0 V), the device M_5 is switched off, blocking the oscillator's signal V_{LO} from reaching the output V_{OUT}. When the impulse voltage level is high (V_{dd}=1.2 V), the signal is passed to the output with minimum loss. This in effect performs the desired envelope shaping as the pulse varies with time. The size of M_5 affects the performance of this circuit considerably, and a device width W of 8 μm gives a good trade-off between insertion loss, bandwidth, and attenuation range.

The envelope shaping performed by the variable attenuator can be analyzed by first considering the drain–source current I_{ds} through the NMOS device M_5. When the gate control voltage V_{ctrl} is less than the device threshold voltage V_t, the device operates in the subthreshold or weak inversion region and the current is given by [37]

$$I_{\mathrm{ds}} \approx I_{\mathrm{S}} e^{\frac{V_{\mathrm{ctrl}}}{nkT/q}} \left(1 - e^{\frac{V_{\mathrm{ds}}}{kT/q}}\right) \tag{11}$$

where I_S and n are empirical fitting parameters with values of 2.4 nA and 1.4, respectively, for the 0.13-μm CMOS technology used and the chosen device width W of 8 μm. Equation (11) amounts to a relatively small subthreshold current I_{ds}, yielding a large device resistance compared with the 50-Ω load. This results in negligible signal transmission from the input to the output, and this mode of operation can thus be ignored.

However, when the gate control voltage V_{ctrl} exceeds the device threshold voltage V_{t}, the device enters the triode region of operation [37]:

$$I_{\mathrm{ds}} \approx \frac{\mu C_{\mathrm{ox}}}{1 + V_{\mathrm{ds}}/LE_{\mathrm{sat}}} \frac{W}{L} \left[(V_{\mathrm{ctrl}} - V_{\mathrm{t}})V_{\mathrm{ds}} - \frac{V_{\mathrm{ds}}^2}{2}\right] \tag{12}$$

Therefore, the resistance R_{ds} of M_5 is approximately

$$R_{\mathrm{ds}} \approx \frac{V_{\mathrm{ds}}}{I_{\mathrm{ds}}} = \frac{1 + V_{\mathrm{ds}}/LE_{\mathrm{sat}}}{\mu C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{ctrl}} - V_{\mathrm{t}} - V_{\mathrm{ds}}/2)} \tag{13}$$

which is a function of the gate control voltage V_{ctrl} and the drain–source voltage V_{ds} across the device

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M_5. It varies from $1/[\mu C_{ox}W/L(V_{ctrl}-V_t)]$ to $2/[\mu C_{ox}W/L(V_{ctrl}-V_t)]$ as V_{ds} varies from 0 V to the velocity saturation drain–source voltage $V_{dsat}=(V_{ctrl}-V_t)\|LE_{sat}$. The average resistance of M_5 with respect to V_{ds} (R_{dsavg}) can be found as:

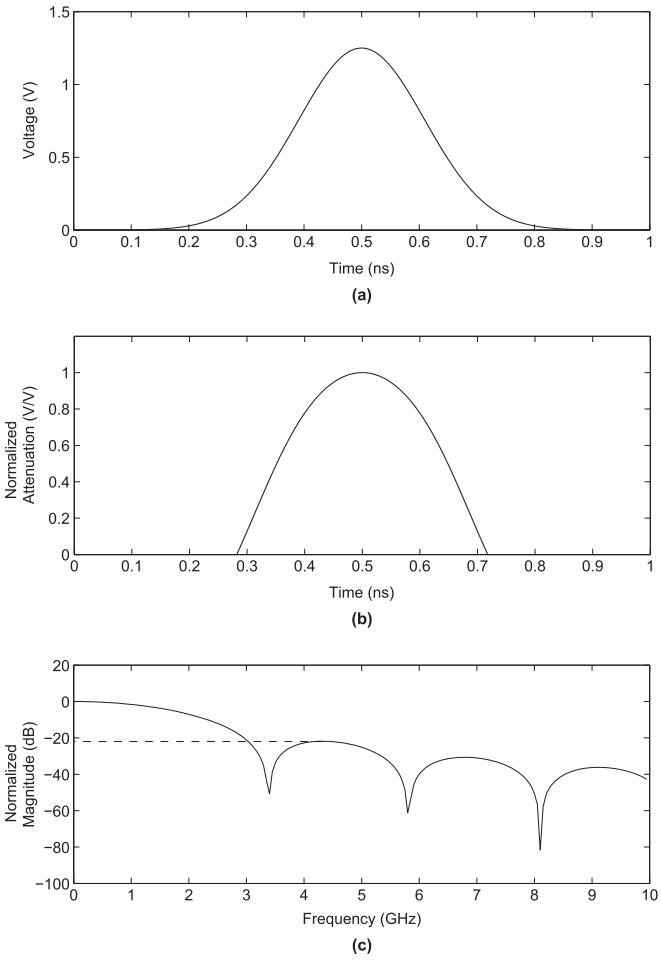

Figure 8. Envelope shaping through variable attenuator: (a) control voltage $V_{ctrl}(t)$, (b) amplitude shaping waveform $T(t)$, and (c) amplitude shaping in frequency domain $|T(j\omega)|$.

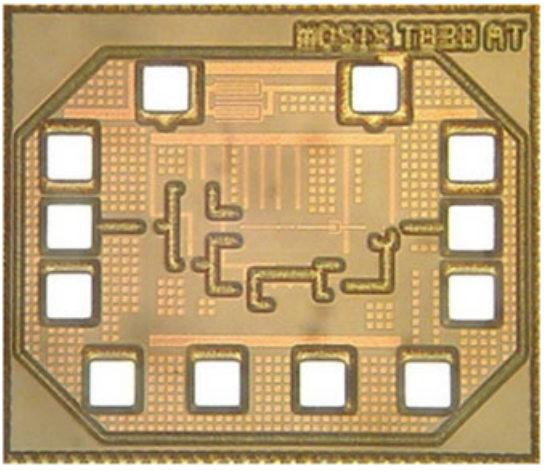

Figure 9. Photograph of ultra-wideband pulse generator IC.

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$$R_{\text{dsavg}} = \frac{\int_0^{V_{\text{dsat}}} R_{\text{ds}} dV_{\text{ds}}}{V_{\text{dsat}} - 0} = \frac{2}{KV_{\text{dsat}}}\left(1 + \frac{2V_{\text{ov}}}{LE_{\text{sat}}}\right)\ln\left|\frac{2V_{\text{ov}}}{2V_{\text{ov}} - V_{\text{dsat}}}\right| - \frac{2}{KLE_{\text{sat}}} \approx \frac{1.5}{KV_{\text{ov}}} \tag{14}$$

where $K=\mu C_{\text{ox}}W/L$ and $V_{\text{ov}}=V_{\text{ctrl}}-V_t$. The transmission coefficient T through the variable attenuator can thus be evaluated as

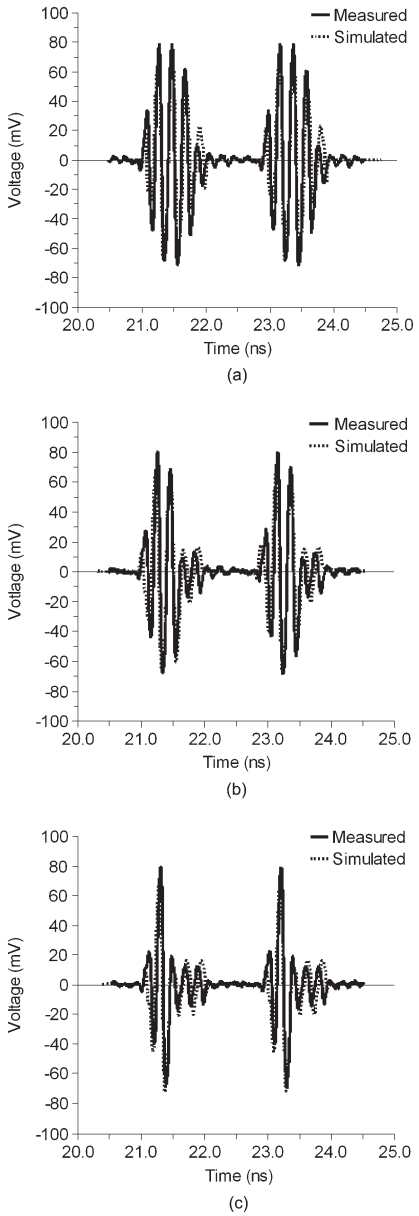

Figure 10. Measured ultra-wideband waveforms at 525MHz pulse repetition frequency with different time durations: (a) long (900ps), (b) moderate (700ps), and (c) short (500ps).

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$$T = \frac{Z_0}{R_{\text{dsavg}} + Z_0} = \frac{\mu C_{\text{ox}}(W/L)Z_0(V_{\text{ctrl}} - V_{\text{t}})}{\mathbf{1.5} + \mu C_{\text{ox}}(W/L)Z_0(V_{\text{ctrl}} - V_{\text{t}})} \tag{15}$$

where Z_0 is the 50-Ω load impedance.

The envelope shaping waveform is computed using Equation (15) for the Gaussian pulse given in Equation (10), with $V_{\text{ctrl}}(t)=p(t)$, and the chosen device width W of 8 μm. Figure 8 shows the control voltage $V_{\text{ctrl}}(t)$, the amplitude shaping waveform $T(t)$, and its Fourier transform $|T(j\omega)|$. It is apparent that the envelope shaping waveform $T(t)$ is different from that of the Gaussian control voltage $V_{\text{ctrl}}(t)$, having a shorter duration and sharper edges due to the nonlinearity of the transfer function T with respect to the control voltage V_{ctrl}. Despite this pulse compression effect, the variable attenuator can theoretically provide 22 dB of out-of-band rejection as evident in Figure 8(c). In simulation, the out-of-band rejection is more than 20 dB using the generated impulse shown in Figure 6 for V_{ctrl}. The series capacitor C_f shown in

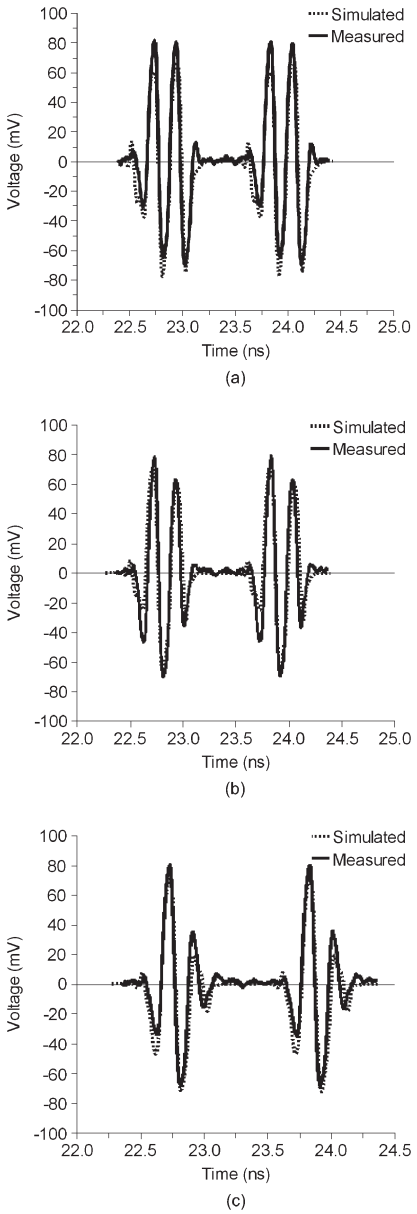

Figure 11. Measured ultra-wideband waveforms at 910 MHz pulse repetition frequency with different time durations: (a) long (600 ps), (b) moderate (525 ps), and (c) short (500 ps).

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Figure 1(b) also acts as a high-pass filter and provides additional rejection of low-frequency components. This relaxes the filtering requirements for meeting the FCC mask, especially in the 1- to 1.6-GHz band where tight limits are imposed for GPS.

3. MEASUREMENT AND SIMULATION RESULTS

The pulse generator was fabricated in a standard 0.13-μm CMOS process, and a photograph of the Integrated Circuit (IC) is shown in Figure 9. It occupies a die area of $725 \times 600\ \mu m^2$ including bonding pads, decoupling capacitors, and the chip guard ring (plus chamfer regions), whereas the core circuit area is only $360 \times 200\,\mu m^2$. The circuit consumes less than 3.8 mW of average power (P_{AVG}) at a PRF of 910 MHz. This gives an energy consumption E_p of less than 4.2 pJ over the pulse repetition time of 1.1 ns:

$$E_p = P_{AVG} \times PRT = P_{AVG}/PRF = 4.2\ pJ \tag{16}$$

The UWB pulse generator IC was measured directly on-wafer using 40-GHz coplanar waveguide probes and DC probes. A 60-GHz Tektronix Digital Serial Analyzer (DSA8200) (Tektronix, Inc. Beaverton, OR United States) was used to observe the pulses in the time domain, whereas a 50-GHz Agilent spectrum analyzer (E4448A) (Agilent Technologies, Inc. Santa Clara, CA United States) was used to examine the output power spectrum. The input clock is a periodic sinusoidal signal that is converted on-chip into a digital square wave using the edge sharpening inverters (Figure 1).

Figures 10 and 11 illustrate the generated UWB waveforms at 525 and 910 MHz PRFs, respectively. The pulses have a peak-to-peak voltage amplitude (V_{pp}) of about 150 mV and a maximum ringing level of −15 dB, with good symmetry about the 0 V (ground) level $(V_{pk+} + V_{pk-})/(V_{pk+} - V_{pk-}) \approx 5.5\%$. The pulse duration can also be tuned over a wide range from about 500 to 900 ps. There is also good agreement between simulated and measured waveforms as observed on the plots.

Figures 12 and 13 show the average power spectrum for the waveforms in Figure 10(c) and Figure 11(c) with a resolution bandwidth of 1 MHz and a frequency span of 10 GHz. The power spectra exhibit well-defined peaks at multiples of the PRF because the output is a periodic (unmodulated) extension of the pulses. Figure 14 shows the pulse power spectra computed from the pulse waveforms in Figure 11 with a frequency resolution of 1 MHz and a span of 10 GHz. It is clear that the −10 dB bandwidth of the pulses varies from about 2 to 3 GHz and that the center frequency is about 4.8 GHz, which corresponds to the ring oscillator's signal frequency. The spectrum roll off is also quite sharp, with more than 25 dB of out-of-band rejection relative to the peak power level. Furthermore, only little attenuation is needed below 3 GHz to ensure compliance with the indoor and/or outdoor FCC masks.

The ring oscillator's oscillation frequency and thus the output pulse center frequency may drift because of changes in process, temperature, and supply voltage. A statistical Monte Carlo simulation

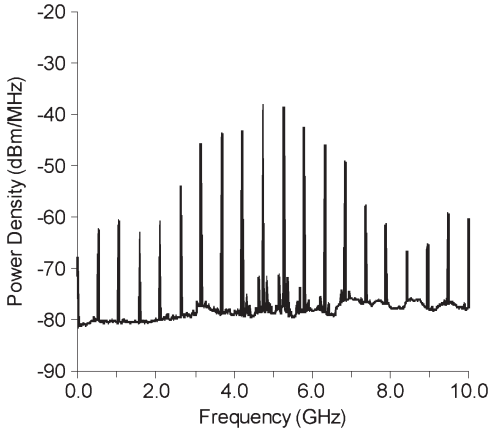

Figure 12. Measured power spectrum at 525 MHz pulse repetition frequency.

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of $N=100$ trials with variations in the process (e.g., device width W, length L, and threshold voltage V_t) for the output center frequency is shown in Figure 15. It is apparent that the center frequency has a mean of 4.8 GHz and a standard deviation of ± 0.31 GHz or approximately $\pm 6\%$. Simulations of the center frequency as a function of temperature and power supply voltage are also shown in Figure 16. As the temperature changes from 0 to 75 °C at the nominal supply voltage of 1.2 V, the pulse center frequency shows a variation of less than $\pm 4\%$ (Figure 16(a)). In addition, the pulse center frequency changes by about $\pm 5\%$ (Figure 16(b)) as the power supply voltage changes by $\pm 5\%$ (from 1.15 to 1.25 V) at the nominal temperature of 25 °C. These variations should be tolerable because they are relatively small compared with the pulse frequency bandwidth of more than 2 GHz or 40%. The integrated power lost into adjacent channels over a 2-GHz bandwidth would be relatively small, and the receiver would still be able to detect the pulse to a certain extent.

Table I summarizes the proposed pulse generator's performance in comparison with other work that has been reported recently. Although it can be difficult to make fair comparisons when different specifications and technologies are used, it is clear that the proposed circuit achieves a relatively low energy consumption of 4.2 pJ/pulse. It is important to note that the low energy consumption of 2.5 and 9 pJ/pulse reported in Refs [26] and [29] does not include 6 and 3.2 mW of power consumed in the output buffer and MOS current mode logic gates, respectively. The proposed pulse generator is also more efficient than most of the other designs if the total energy consumption per pulse is normalized with respect to the output peak-to-peak voltage.

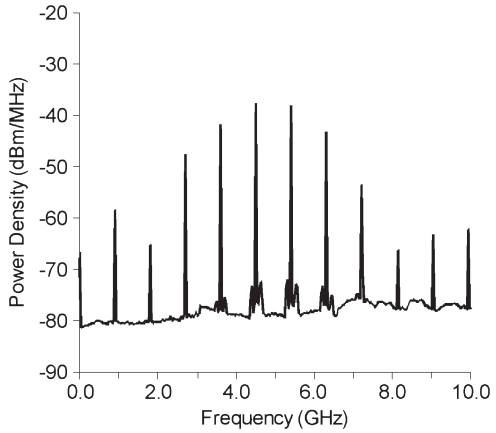

Figure 13. Measured power spectrum at 910 MHz pulse repetition frequency.

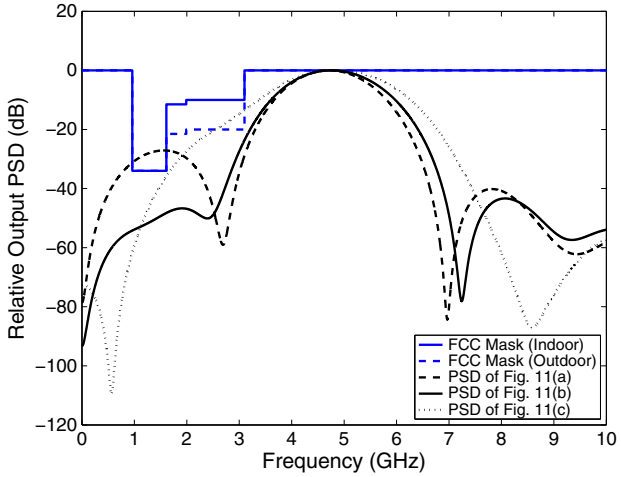

Figure 14. Computed pulse frequency spectrum for the waveforms in Fig. 11.

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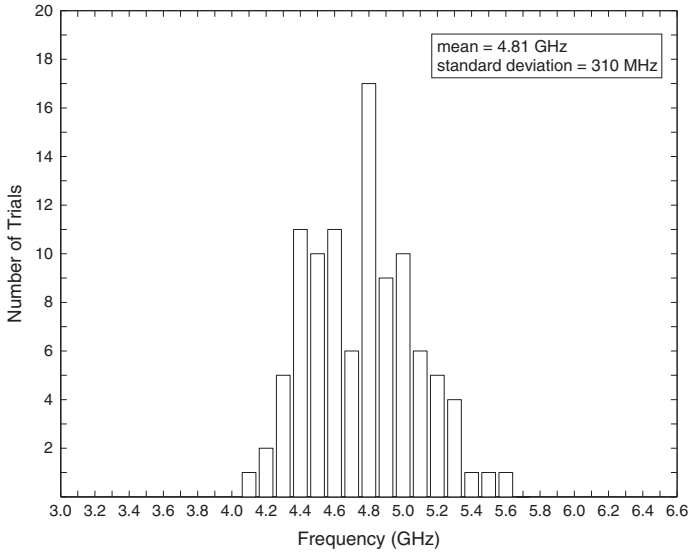

Figure 15. Statistical Monte Carlo simulation of the oscillator center frequency with process variations.

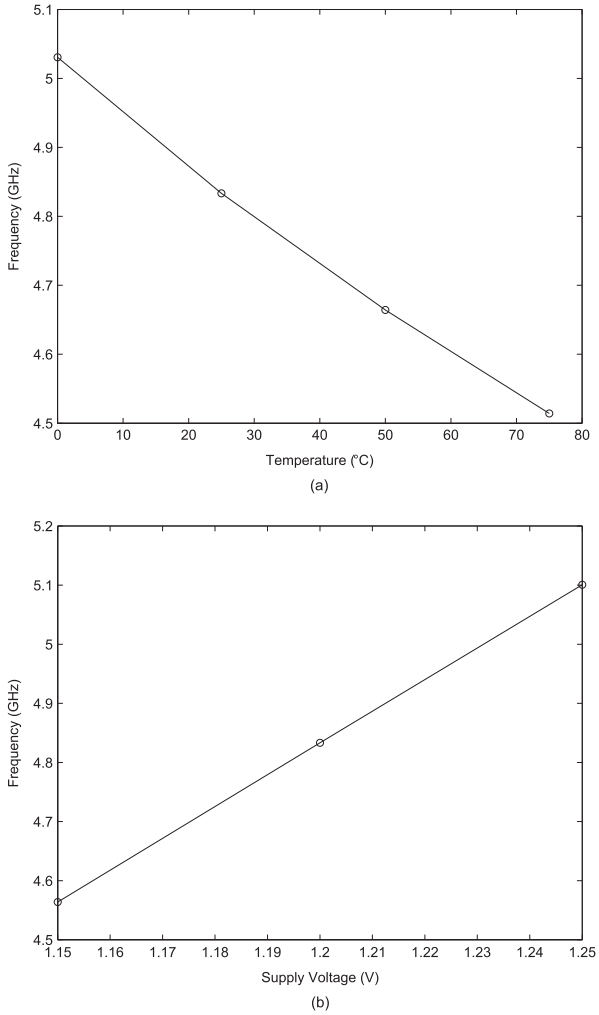

Figure 16. Variation of the oscillator center frequency with (a) temperature and (b) supply voltage.

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Table I. Summary of pulse generator's performance in comparison with other work.

	Technology	Supply (V)	Power (mW)	PRF (MHz)	Energy (pJ/p)	Pulse amplitude	Pulse duration (ns)
[4]	90-nm CMOS	1.0	129	1800	–	220 mV	0.53
[7]	0.18-μm CMOS	1.8	76	400	–	195 mV	<1.0
[8]	0.18-μm CMOS	1.8	–	750	2	30 mV	0.5
[9]	0.18-μm CMOS	1.8	–	500	0.56	–	1.0
[11]	0.18-μm CMOS	1.8	12.6	1160	–	123 mV	0.28
[13][a]	90-nm CMOS	1.0	3.0	5000	–	200 mV	0.045
[26]	0.35-μm SiGe BiCMOS	2.4	2.5[b]	1000	2.5[b]	300 mV	0.6
[29]	0.13-μm CMOS	1.2	3.84	100	9[c]	1.42 V	0.46
[32]	0.18-μm CMOS	–	50	1000	50	110 mV	0.14–1.0
[33]	0.18-μm CMOS	–	–	2500	25	80 mV	0.12 to >1.0
This work	0.13-μm CMOS	1.2	3.8	910	4.2	150 mV	0.5–0.9

[a]Simulation results.
[b]Does not include 6 mW of power in output buffer.
[c]Does not include 3.2 mW of power in MOS current mode logic gates.

4. CONCLUSIONS

A new energy-efficient tunable pulse generator has been developed in 0.13-μm CMOS for high-data-rate 3.1- to 10.6-GHz UWB applications. A current-starved ring oscillator is quickly switched on and off for the pulse duration, and the amplitude envelope is shaped using a variable passive CMOS attenuator. The attenuator is controlled with an impulse, which is created by a low-power, tunable glitch generator (CMOS NOR gate). Several UWB pulses were measured and demonstrated, with the pulse duration varying over a wide range (500–900 ps). The spectrum roll-off is also quite sharp with high out-of-band rejection to help satisfy the FCC mask. The entire circuit operates in switched mode with a low average power consumption of less than 3.8 mW at 910 MHz PRF or below 4.2 pJ of energy per pulse. It occupies a total area of 725×600 μm^2, including bonding pads and decoupling capacitors, and the active circuit area is only 360×200 μm^2.

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