Active quasi-circulator with high port-to-port isolation and small area

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An active quasi-circulator integrated circuit relying on a differential central core is presented. Measurements on the quasi-circulator reveal that the forward transmission coefficients, S_{21} and S_{32}, are both close to −4 dB in the range of 2.5 to 6 GHz. The isolation between the ports is greater than 20 dB and can reach up to 59 dB in the case of S_{13}. The chip was fabricated on a standard 130 nm CMOS process and the core circuit area measures 0.105 mm^2, making it the smallest active quasi-circulator known to date.

Introduction: A considerable number of active quasi-circulator circuits have been demonstrated to date in both hybrid and RFIC form [1–6]. A key reason to use an active quasi-circulator compared to a passive ferrite-based one is to reduce cost. Hybrid and RFIC implementations have their own respective advantages in relation to cost and which circuit is seleted is dependent on the end-use of the quasi-circulator. For medium-power applications, for example, a hybrid circuit might be a better solution than an RFIC implementation because relatively inexpensive packaged power transistors can be easily found. Of course, one drawback of the hybrid circuit is its large area. For small-signal applications, a general-purpose RFIC quasi-circulator can be the more cost-effective choice. In this Letter, we report a quasi-circulator CMOS RFIC that relies on a novel differential circuit topology. A pair of transconductor circuits are used to convert differential voltage signals to current signals which can be summed to provide isolation between two of the ports. This quasi-circulator has the smallest active area known to date, measuring only 0.105 mm^2.

Quasi-circulator circuit: A schematic diagram of the proposed quasi-circulator is shown in Fig. 1. First, note that the circuit accepts a differential signal at port 1 while ports 2 and 3 are single-ended. The in-phase component at port 1 passes through a common-gate NMOS device, M_1, and exits at port 2. When a signal is incident at port 2 the signal will travel in the forward direction through the top transconductor circuit (g_m) and exit at port 3.

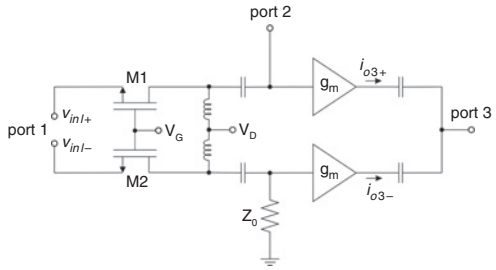

Fig. 1 *CMOS quasi-circulator schematic diagram*

Next, consider the port-to-port isolations. The incident RF signal at port 1 sees a symmetric circuit structure as it propagates through the circuit until it reaches the output node at port 3. The shunt load impedance, Z_0, located on the bottom branch, has the same value as the characteristic impedance seen at port 2 to preserve the symmetry. The differential voltage signal that originates at port 1 is converted to differential currents by identical transconductor circuits. When the currents are summed at port 3 they cancel each other out because they are out-of-phase and this is how port 1 and port 3 are isolated from each other. A signal incident at port 2 encounters a high impedance at M_1 because it enters the transistor at the drain and this provides the reverse isolation between ports 2 and 1. A signal incident at port 3 encounters the transconductor circuits in reverse as well as the common-gate transistors M_1 and M_2. Therefore, we expect the isolation from port 3 to port 1 (S_{13}) to be the highest of all and the port 3 to port 2 isolation (S_{23}) to be second highest, which is confirmed by experiment.

The transconductor block used in the quasi-circulator to convert from voltage to current is shown in Fig. 2. The circuit has two distinct parts: a buffer stage and a transconductance stage. The transonconductance stage consists of transistors M_3 to M_5. Transistor M_4 is in a cascode arrangement relative to M_3 and its purpose is to mitigate the Miller effect in device M_3 and thereby extend its frequency response. The output signal current is taken at the drain of M_4. Note that M_5 is a PMOS device and it is used as a current source and active load. The resistor R_7 is a feedback resistor to obtain a wide frequency response with the PMOS device. In principle, a cascode device can be used with the M_5 PMOS transistor to make the circuit symmetric with the NMOS part. Nevertheless, that option was not pursued because having four transistors stacked on top of each other, all biased from a single 1.2 V supply at the top, would have reduced the voltage headroom of the transistors to an unacceptably low level.

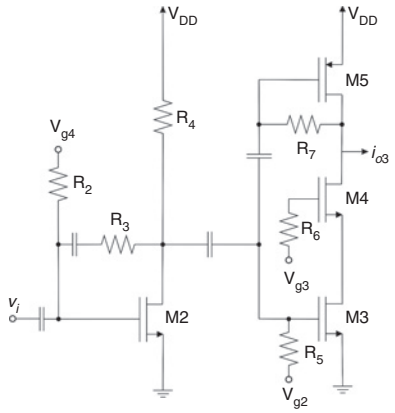

Fig. 2 *Transconductance stage*

The input impedance to the transconductance stage in Fig. 2 is high and therefore some type of matching circuit is necessary to avoid a high reflection coefficient at port 2. The solution chosen in this design was to insert a buffer stage with a moderately low input impedance ahead of the transconductance stage. The buffer is a simple common-source amplifier with resistive feedback. Although the buffer increases the DC power consumption of the chip, it is capable of providing a reasonably low reflection coefficient over a wide frequency band and, furthermore, it takes up a very small amount of area compared to the alternative of using a tuned, passive, matching network.

Experimental results: To demonstrate the quasi-circulator concept, a chip was fabricated using a standard 130 nm CMOS process from IBM. Small-signal, large-signal and noise figure measurements were carried carried out directly on-wafer.

Fig. 3 shows the measured forward transmission between the ports of the quasi-circulator together with a microphotograph of the chip. The forward transmission coefficients both have good flatness: S_{21} is -3.8 ± 0.4 dB and S_{32} is -4.3 ± 0.79 dB over the measured frequency band of 2.5 to 6.0 GHz. The maximum difference between the forward coefficients, $|S_{21} - S_{32}|$, over frequency was 1 dB. The reflection coefficients at the three ports of the quasi-circulator are shown in Fig. 4. The best match is observed at port 2, while the worst-case match is at port 3.

The measured port-to-port isolations are shown in Fig. 5. The port 1 to port 3 isolation, S_{31}, is typically the most challenging to reduce in the active quasi-circulator design because it is in the forward path of the signal flow. In this chip, the S_{31} isolation is obtained through signal cancellation and it is between 20 and 21 dB, a result that compares well with other quasi-circulators reported in the literature (see Table 1). The port 2 to port 1 isolation, S_{21}, was between 23.4 and 24.5 dB, while the port 3 to 2 isolation, S_{23}, was between 30.6 and 40.3 dB. The best isolation, as expected, was from port 3 to port 1 (S_{13}) with a value between 42.7 and 59 dB over the measured frequency band.

RF power measurements were carried out at 6 GHz. With the incident signal applied at port 1 and the output taken at port 2, the IP_{1dB} was measured at +3 dBm. In addition, a two-tone test was done with the centre frequency at 6 GHz and a tone spacing of 1 MHz. The two-test revealed an IIP_3 from port 1 to port 2 of +16.9 dBm. Lastly, noise figure (NF) measurements were also conducted and the average NF from port 1 to port 2 was 14 dB while for port 2 to 3 it was between 6 and 8 dB over the frequency span of 2.5 to 6 GHz.

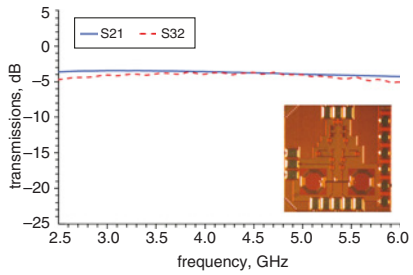

Fig. 3 *Measured transmission losses and chip microphotograph*

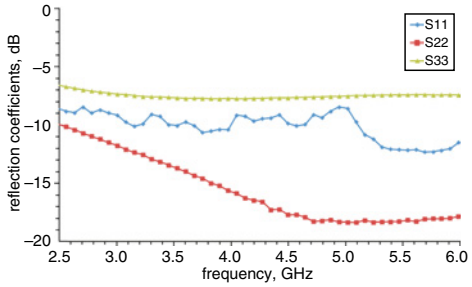

Fig. 4 *Measured reflection coefficients*

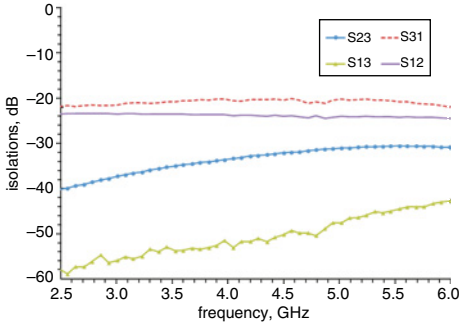

Fig. 5 *Measured port-to-port isolations*

Table 1: Summary and comparison table

Frequency (GHz)	This work	[2]	[4]	[5]
	2.5–6	29–31	1.5–2.7	1.5–9.6
Size (mm^2)	0.105	0.36	0.25	0.41
IP_{1dB} (dBm)	+3	−7	−6.4	−3.7
Power (mW)	66	15	86	31.6
S_{21} (dB)	−3.8 ± 0.4	− 4 to −6	2.4 to 1.5	−5 ± 1
S_{32} (dB)	−4.3 ± 0.79	−7.2 to −7.9	0 to −3	−5 ± 1
S_{31} (dB)	>20	>12	>26	>18
S_{12} (dB)	>23	>24	>25	>30
S_{23} (dB)	>31	>22	>25	>17
S_{13} (dB)	> 43	> 35	> 21	> 40

Conclusion: A new active quasi-circulator has been demonstrated in which the forward isolation between ports 1 and 3 is obtained through the use of signal cancellation. The cancellation is realised by converting the differential voltage signal at port 1 to current signals and then adding them together at the output node. The chip exhibits excellent isolation between all of the ports and the forward insertion loss from ports 1 to 2 and from ports 2 to 3 has good flatness.

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One or more of the Figures in this Letter are available in colour online.

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