A Quadrature Pulse Generator for Short-Range UWB Vehicular Radar Applications Using a Pulsed Oscillator and a Variable Attenuator

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***Abstract*—A new quadrature tunable pulse generator is presented in this paper using 0.13 μm CMOS for 22–29 GHz ultrawideband (UWB) vehicular radar. A quadrature inductor-capacitor (LC) oscillator is quickly switched on and off for the duration of the pulse, and the amplitude envelope is modulated with an impulse using a variable passive CMOS attenuator. The impulse is realized using a glitch generator (CMOS NAND gate) and its duration can be changed over a wide range (375 ps to more than 1 ns). The switching technique used in the quadrature oscillator creates a large initial voltage for fast startup (0.5 ns) and locks the initial phase of the oscillations to the input clock for pulse coherence. The measured phase noise thus matches that of the clock signal, with a relatively low phase noise of −70 dBc/Hz and −100 dBc/Hz at 1kHz and 1 MHz offsets respectively. The entire circuit operates in switched-mode with a low average power consumption of less than 2.2 mW and 14.8 mW at 50 MHz and 600 MHz pulse repetition frequencies, or below 11 pJ of energy for each of the four differential quadrature pulses. It occupies an active area of less than 0.41 mm^2.**

***Index Terms*—CMOS integrated circuits, pulse generator, ultrawideband, vehicular radar.**

I. Introduction

THE FREQUENCY spectrum from 22 GHz to 29 GHz was made available by the U.S. Federal Communications Commission (FCC) for short-range radar (SRR) systems on terrestrial transportation vehicles [1]. Such systems are able to detect the location and movement of objects near a vehicle by developing a 360° radar map of its surroundings, to provide safety features such as near collision avoidance, enhanced airbag activation, and improved suspension system control that better responds to road conditions [1], [2]. Normally, the average power spectral density (PSD) should not exceed −41.3 dBm/MHz to avoid interference [1], affecting the introduction of vehicular radars in the U.S. and global markets, and having a significant impact on system and pulse waveform design.

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UWB SRR is considered a key element in comprehensive environment sensing for automobiles, complementing other technologies such as infrared (IR), ultrasonic, video, and long-range active cruise control (ACC) radars [2]. A network of 16 or more UWB radar sensors around the vehicle [3] can provide a variety of features to improve passenger safety, ranging from simple parking aids to more sophisticated blind-spot monitoring, precrash detection, and stop-and-go or short-range cruise control. Such applications require a high resolution of about 10 cm. Increasing the number of radar sensors can increase the processing capability and reliability of the SRR system.

Pulsed UWB technology is based on the transmission of short pulses with subnanosecond time duration, thereby spreading the signal bandwidth over several gigahertz. Pulsed UWB techniques potentially offer several advantages over conventional radar approaches, including higher range resolution, enhanced target radar cross section (RCS) and identification, increased immunity to passive interference (e.g., rain), and the ability to detect very slowly moving targets. [4], [5]. Their transceiver architecture is also one of the simplest to implement, potentially making them very cost-effective. Furthermore, time-gating can increase isolation between the transmitter and receiver for a longer operating range, and low duty cycling can significantly reduce the power consumption.

In conventional pulsed vehicular radars [2], [6]–[16], pulses are generated by time gating the output of a high-frequency local oscillator (LO) phase-locked loop (PLL) using a switch. The output amplitude envelope typically has a rectangular shape, which results in an inefficient sinc spectrum with high out-of-band power that will need to be filtered [17]. The LO PLL is also continuously running since its turn-on and locking transient are usually not short enough for it to be switched off and on during the interpulse period, resulting in high LO leakage and a low power efficiency. Furthermore the LO PLL can be rather complex, consuming a significant amount of power. Even though power consumption is not a primary concern in automobile applications, the total power consumption can become significant as the number of sensors increases [18]. Pulsed or gated local oscillators have been investigated to reduce LO leakage, circuit complexity, and power consumption [19]–[26]. However, the oscillator turn-on and stabilization time can be relatively long, limiting the pulse duration and bandwidth. In addition, there is little control over the startup and turn off transients and the output pulse shape cannot be readily tuned. Other pulse generators have been reported that use passive filters [27] or distributed structures of edge combiners [18]. They are often lim-

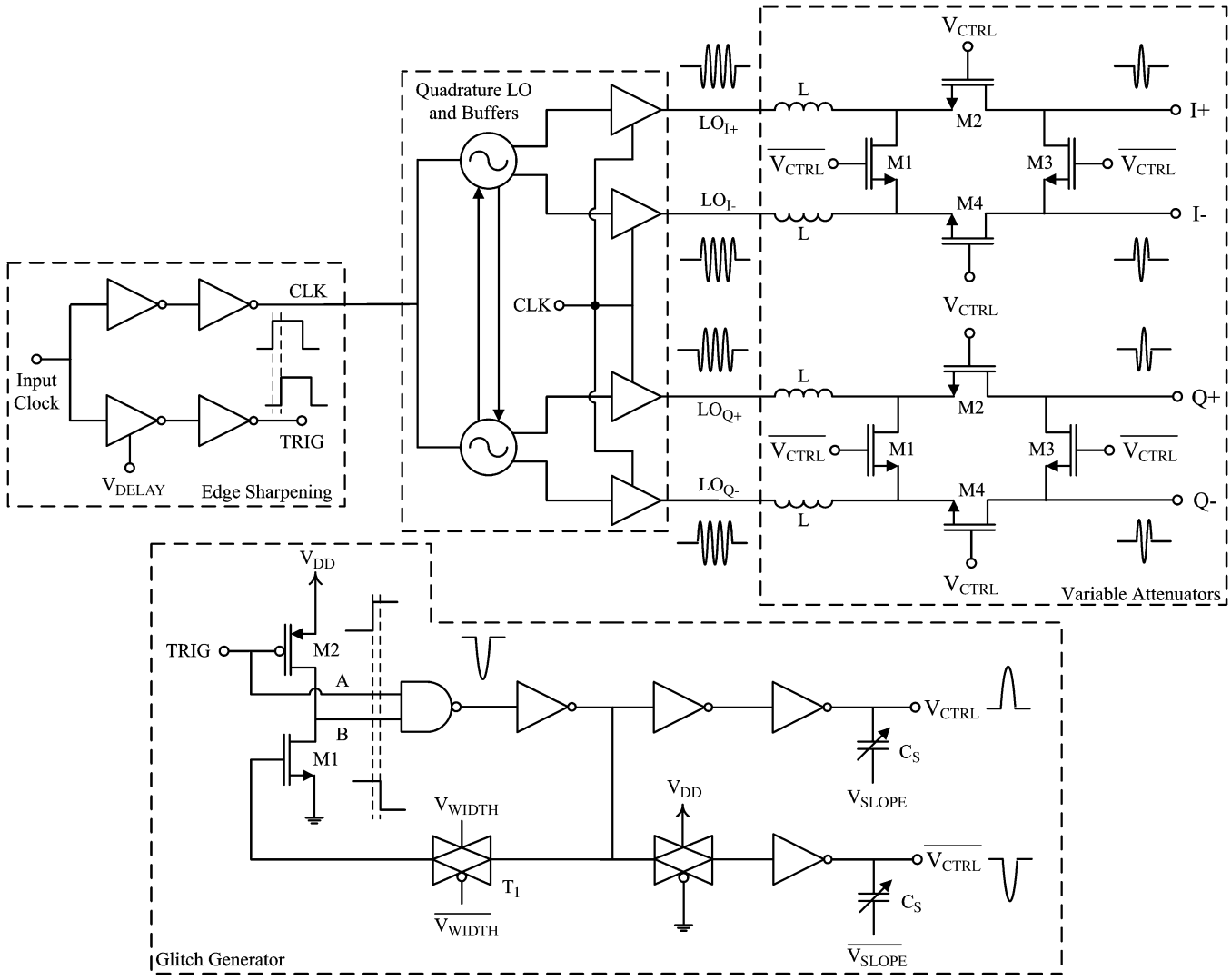

Fig. 1. Proposed UWB pulse generator circuit diagram.

ited to a specific pulse shape and frequency spectrum that highly depend on device parameters and matching, and are difficult to control to handle process variations, regulatory differences, and changes in the channel or antenna characteristics.

In this paper, a new quadrature pulse generator is proposed in 0.13 μm CMOS for short-range 22–29 GHz UWB vehicular radar. It can be used in pulsed UWB vehicular radar transceivers to provide template pulses for quadrature pulse correlation and detection [2], [8], [28], [29], or to enable quadri-phase coding for enhanced pulse compression, detection, and interference mitigation. A quadrature inductor-capacitor (LC) oscillator operating at 24 GHz is used in this work, which can be switched off between pulses to reduce LO leakage, LO self mixing, dc offsets, and power consumption. The oscillator switching technique injects a current impulse upon startup with a short time duration and large harmonic components out to 24 GHz, creating a large initial condition for a short settling time of about 0.5 ns, and locking the initial phase of the oscillations to the input clock for high pulse-to-pulse coherence. The measured output phase noise matches that of the clock signal, yielding a relatively low phase noise of -70 dBc/Hz at 1 kHz offset, and -100 dBc/Hz at 1 MHz offset. This amounts to a low integrated rms jitter from 100 Hz to 1 MHz of less than 720 fs. A π-network attenuator then modulates the LO signal to generate the UWB pulse. The attenuator is controlled with two inverted impulses, which can be readily tuned to vary the width of the UWB pulse over a wide range from 375 ps to more than 1 ns. Such an approach provides good control of the radiated frequency spectrum, as the -10 dB bandwidth can reach 4.9 GHz and the out-of-band rejection can exceed 23 dB. The pulse generator can operate with a pulse repetition frequency (PRF) as high as 600 MHz, allowing it to be readily shared between the transmitter and receiver with a time delay as short as 1.66 ns. The circuit is fully differential and operates in switched mode with zero static current for a low power consumption of only 2.2 mW and 14.8 mW at PRFs of 50 MHz and 600 MHz respectively, or less than 11 pJ of energy for each of the four differential quadrature pulses. The integrated circuit (IC) occupies a die area of 0.94 mm^2 including bonding pads and decoupling capacitors, and the active circuit area is only 0.41 mm^2.

II. Circuit Architecture and Design

A circuit schematic of the 22–29 GHz UWB pulse generator is shown in Fig. 1. It consists of a quadrature LC local oscillator

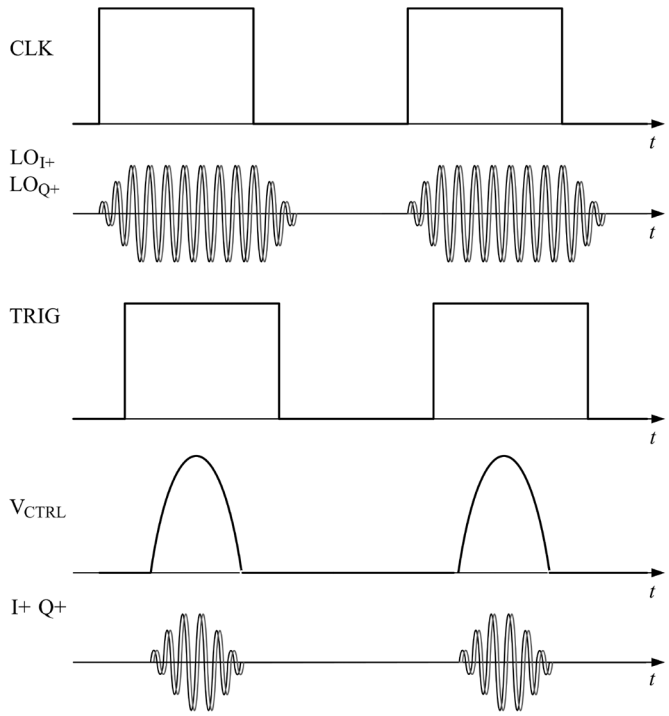

Fig. 2. Pulse generator clock timing and output waveforms.

(LO), buffers, a glitch generator and variable π-network attenuators. An inverter chain first sharpens the rising/falling edge of the clock signal (CLK), which is used to turn the LO and buffers on and off. The clock signal (TRIG) then triggers the glitch generator, where a NAND gate operates on the rising-edge and its delayed inverse to form a short impulse ($V_{\rm CTRL}$). This impulse and its inverse control the variable π-network attenuator to shape the amplitude envelope of the LO signals ($\rm LO_{I+}, LO_{I-}, LO_{Q+}, LO_{Q-}$) and form the desired quadrature UWB pulses at the outputs ($I+, I-, Q+, Q-$). Fig. 2 illustrates the timing of the clock signals (CLK, TRIG) and the generated pulse waveforms. Note that the glitch generator clock signal (TRIG) is delayed with respect to the LO's clock signal (CLK) using current-starved inverters (Fig. 1). This in turn delays the onset of $V_{\rm CTRL}$, allowing sufficient time for the oscillations to stabilize and reach steady state before amplitude shaping takes place. The delay between TRIG and CLK can be tuned using the control voltage $V_{\rm DELAY}$ (Fig. 1).

A. Pulsed Quadrature LC Oscillator

A common way of implementing a differential LC oscillator is to use a cross-coupled pair of transistors to generate the negative resistance required and overcome the losses in the LC tank. The resistance $R_{\rm IN}$ seen looking into the cross-coupled pair is given by $-2/g_m$, where g_m is the transconductance of each of the transistors. Therefore, with sufficient device size and biasing current, a negative resistance larger than the equivalent parallel resistance of the tank (R_P) can be realized to sustain the oscillations.

The quadrature LC oscillator circuit designed in this work is shown in Fig. 3. It consists of two cross-coupled oscillators that are connected together through the body terminals (or backgates) of the PMOS devices M_{P1}, M_{P2}, M_{P3} and M_{P4}. Adding cross-coupled PMOS transistors ($M_{P1}-M_{P2}$ and $M_{P3}-M_{P4}$) above the cross-coupled NMOS transistors ($M_{N1}-M_{N2}$ and $M_{N3}-M_{N4}$) increases the transconductance per unit current (g_m/I) for a low power consumption. It also improves the symmetry and phase noise of the oscillations as shown in [30], [31]. Quadrature-coupling the two oscillators using the body terminals of the core PMOS devices saves power as opposed to using additional transistors which will also add noise [32], [33]. The resistors R_B are added for dc biasing of the body terminals and the capacitors C_B for ac coupling. The free-running oscillation frequency ω_0 for each oscillator is specified by the resonant frequency of the LC tank $1/\sqrt{\rm LC}$, where L is the value of the on-chip spiral inductor and C is the total parasitic capacitance at the output nodes. The inductors used in this circuit are symmetric spirals, and are 100 μm $\times$ 100 μm in size with one turn and 7.5 μm trace width. An electromagnetic (EM) simulation of the inductors predicts an inductance of 0.16 nH and a quality-factor (Q) of approximately 26 at 24 GHz. The total capacitance C including the parasitic capacitance of the cross-coupled transistors, common-source buffers ($M_{N5}-M_{P5}$, $M_{N6}-M_{P6}$, $M_{N7}-M_{P7}$, and $M_{N8}-M_{P8}$) and metal interconnects is about 0.27 pF to provide oscillation at 24 GHz.

The initial startup transient of the oscillations can be characterized by the well-known "van der Pol" nonlinear differential equation [34] given by

$$\ddot{v} + \epsilon\omega_0[v^2 - 1]\dot{v} + \omega_0^2 v = 0 \tag{1}$$

where $\epsilon = (g_m - 1/R_P)\sqrt{L/C}$ is a damping factor. An approximate solution to (1) for the differential output voltage v can be found as [35]

$$v(t) = \frac{2v_0}{\sqrt{1 + \left(\left(\frac{2v_0}{v(0)}\right)^2 - 1\right)e^{-\epsilon\omega_0 t}}}\cos(\omega_0 t - \phi) \tag{2}$$

where $v(0)$ is the initial condition and $2v_0$ is the steady-state oscillation amplitude. The oscillation phase ϕ depends on the initial conditions. The settling time t_s for the oscillation $v(t)$ to reach 90% of its steady state value $(2v_0)$ can be derived from (2) [35]

$$t_s \approx \frac{Q_{\rm res}}{\omega_0(A_{\rm OL} - 1)}\left[2\ln\left(\frac{2v_0}{v(0)} - 1\right) + 1.45\right] \tag{3}$$

where $A_{\rm OL} = g_m R_P$ is the open-loop gain and $Q_{\rm res} = R_P\sqrt{C/L}$ is the quality-factor of the LC tank. It is clear that the settling time t_s is shorter for larger initial conditions $v(0)$. In addition, the settling time can be reduced by decreasing $Q_{\rm res}/(\omega_0(A_{\rm OL}-1))$, which can be approximated for $A_{\rm OL} \gg 1$ as:

$$\frac{Q_{\rm res}}{\omega_0(A_{\rm OL} - 1)} \approx \frac{Q_{\rm res}}{\omega_0 A_{\rm OL}} = \frac{R_P\sqrt{C/L}}{g_m R_P/\sqrt{\rm LC}} = \frac{C}{g_m}. \tag{4}$$

From (4), the settling time t_s can be reduced by decreasing the tank capacitance C or increasing the transistor transconductance g_m. Thus, the capacitance C is minimized to include only the parasitic capacitance of the cross-coupled transistors

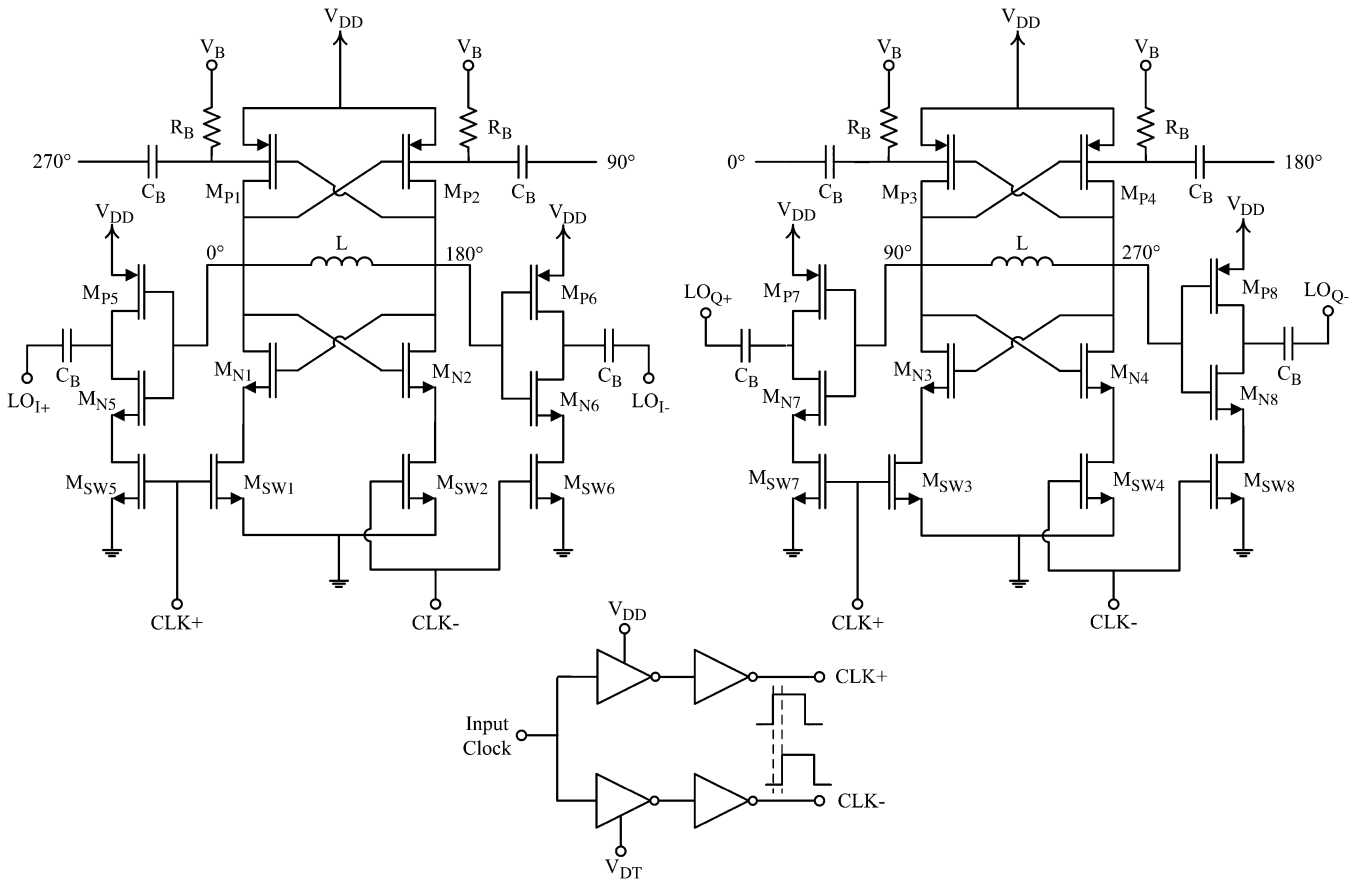

Fig. 3. Circuit schematic of quadrature LC oscillators and buffers.

$(M_{N1}, M_{N2}, M_{P1}, M_{P2})$ and the connecting common-source buffers ($M_{N5} - M_{P5}$ and $M_{N6} - M_{P6}$).

The biasing currents of the two differential oscillators are switched on and off using a pair of NMOS switches ($M_{SW1} - M_{SW2}$ and $M_{SW3} - M_{SW4}$) as shown in Fig. 3. Similarly the biasing currents of the four output common-source buffers are switched using NMOS switches $M_{SW5} - M_{SW6}$ and $M_{SW7} - M_{SW8}$. By switching on one side of each differential oscillator before the other (i.e., switching on M_{SW1} before M_{SW2}, and M_{SW3} before M_{SW4}), a current I_{inj} initially flows through the LC tank as shown in Fig. 4. The current-starved inverters shown in Fig. 3 are used to introduce a short delay between the clock signals CLK+ and CLK− that trigger the pair of switches, and thus the initial current I_{inj} only flows for a short time. In effect, a current impulse with a short time duration and high frequency content out to 24 GHz is injected through the LC tank. This creates a large initial condition $(v(0))$ for a short settling time as indicated by (3) [35]. It also sets the initial phase of the oscillations at the turn-on instant. By setting the same initial oscillation phase at each clock rising edge, the LO pulses are phase coherent with the input clock and pulse-to-pulse coherency is maintained. Note that the delay Δt between the clock signals CLK+ and CLK− can be tuned using the control voltage V_{DT} (Fig. 3) to vary the time duration of the current impulse I_{inj}.

Time-domain simulations of the oscillator differential output voltage $v(t)$ are shown in Fig. 5, with different delays Δt introduced between the clock signals CLK+ and CLK− using the control voltage V_{DT}. The input clock frequency is set to 500 MHz for these simulations. Fig. 5(a) shows the output voltage for $V_{DT} = 0.98$ V and $\Delta\text{t} = 18$ ps in comparison with that obtained for $V_{DT} = V_{DD} = 1.4$ V and $\Delta\text{t} = 0$ ps. It is clear that the settling time is reduced by roughly a factor of 2 when a delay of $\Delta\text{t} = 18$ ps is applied. Fig. 5(b) shows the output voltage with V_{DT} set to 0.8 V, 0.98 V, and 1.2 V, and it is clear

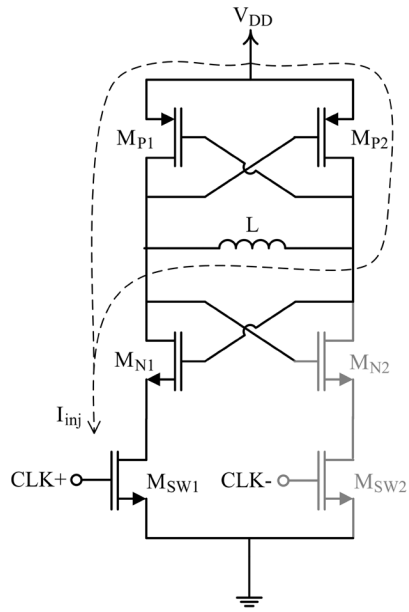

Fig. 4. Illustration of the current injected into the differential LC oscillator.

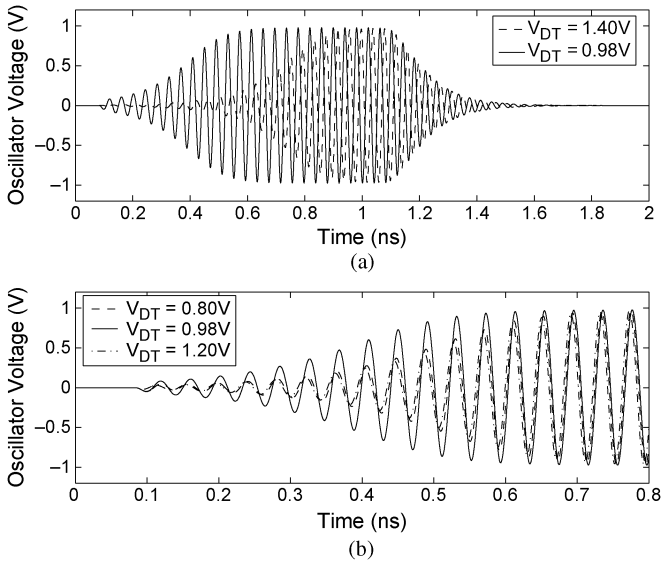

Fig. 5. Simulated oscillator output voltage $v(t)$ for: (a) V_{DT} set to 0.98 V and 1.4 V, and (b) V_{DT} set to 0.8 V, 0.98 V, and 1.2 V.

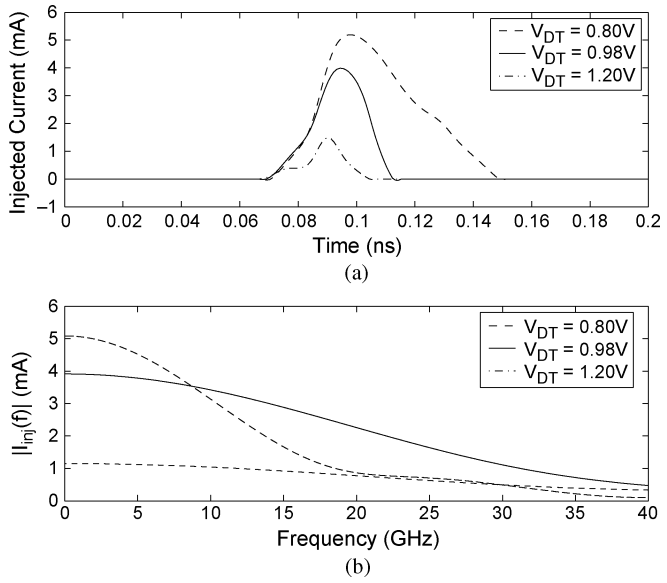

Fig. 6. Simulated injected current impulse $I_{\rm inj}$ for V_{DT} set to 0.8 V, 0.98 V, and 1.2 V. (a) Time-domain waveform. (b) Frequency spectrum.

that the shortest settling time is achieved with $V_{DT} = 0.98$ V and $\Delta t = 18$ ps. The injected current impulse $I_{\rm inj}$ is also illustrated in Fig. 6(a) for the same control voltages, and its frequency spectrum is plotted in Fig. 6(b). The injected current impulse for $V_{DT} = 0.98$ V has an amplitude of 4 mA and a short time duration of about 48 ps. It also has a large frequency component at 24 GHz compared to the injected current impulses for $V_{DT} = 0.8$ V and $V_{DT} = 1.2$ V, yielding a relatively large initial condition voltage $v(0)$ of about 45 mV for the shortest settling time.

Timing diagrams for the clock signals $(\text{CLK}+, \text{CLK}-)$ and the differential quadrature oscillating waveforms ($\text{LO}_I = \text{LO}_{I+} - \text{LO}_{I-}$ and $\text{LO}_Q = \text{LO}_{Q+} - \text{LO}_{Q-}$) are shown in Fig. 7 for $V_{DT} = 0.98$ V. It is clear that the LO signals (LO_I and LO_Q) reach steady state within 0.5 ns from startup (i.e., CLK+ rising edge). The LO remains on for the duration of the clock signal CLK+ when it is in logic 1 to

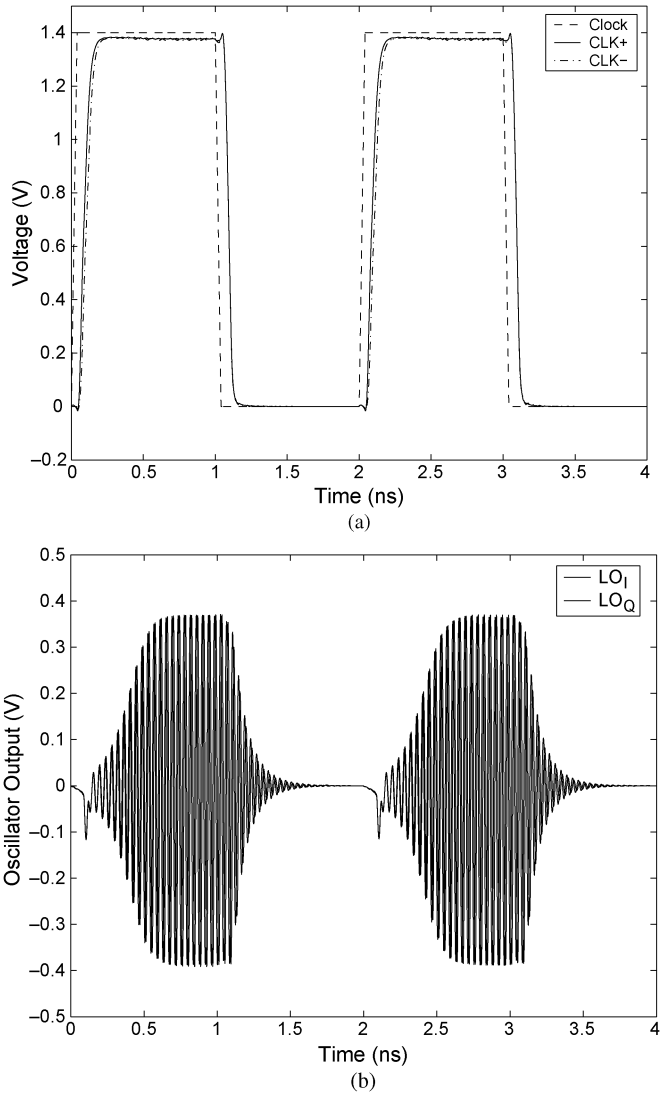

Fig. 7. Simulated timing diagrams for: (a) clock signals and (b) oscillator waveforms.

allow sufficient time for amplitude shaping using the generated impulse signals.

B. Glitch Generator

The subnanosecond glitch generator [12], [36]–[38] shown in Fig. 1 creates a wideband impulse having the required width and shape. The pulse produced is also tunable to allow for different pulse durations and bandwidth. The circuit is implemented using low-power CMOS digital logic, providing full voltage swing required to operate the variable attenuator. A Gaussian-like pulse is created in a glitch fashion by feeding the NAND gate with a clock rising edge along with its delayed inverse (A and B in Fig. 1). The short duration where both signals are high causes the NAND gate's output to be temporarily pulled low thus generating the pulse (Fig. 1). The propagation time through the feedback loop, which consists of the propagation time through the NAND gate, the following inverter and the charging time of transistor M_1, specifies this duration and thus the pulse width. A CMOS transmission gate T_1 is added in the feedback path to control the charging (RC) time constant of transistor M_1. By varying the control voltage

V_{WIDTH}, the charging time-constant changes, which tunes the generated pulse width. Two cascaded inverters serve as a buffer to drive the variable attenuator for the generated pulse V_{CTRL}, while a transmission gate followed by an inverter realize the inverted pulse $\overline{V_{\mathrm{CTRL}}}$. In addition, varactors C_S are connected to the outputs V_{CTRL} and $\overline{V_{\mathrm{CTRL}}}$ as shown in Fig. 1 to vary the loading capacitance and thus tune the rise/fall times (slopes) of the generated pulses. The optimum size for each device is determined by extensive simulation. Simulations indicate that pulses with different time durations can be generated, with the minimum duration being below 400 ps and the maximum duration being bounded by the on period of the clock signal (TRIG). The pulse peak voltage is equal to the supply voltage of $V_{DD} = 1.4$ V for all pulse durations.

C. Variable Attenuator

The variable attenuator consists of two series NMOS devices M_2 and M_4 connected to two shunt NMOS devices M_1 and M_3 in a π-network configuration as shown in Fig. 1. These are driven by the glitch generator pulses V_{CTRL} and $\overline{V_{\mathrm{CTRL}}}$. When V_{CTRL} is low and $\overline{V_{\mathrm{CTRL}}}$ is high, the series NMOS devices are off and the shunt NMOS devices are on, blocking the LC oscillator's signal and shorting the output for maximum attenuation. When V_{CTRL} is high and $\overline{V_{\mathrm{CTRL}}}$ is low, the opposite occurs and the signal is passed to the output with minimum loss. This in effect performs the desired envelope modulation as V_{CTRL} and $\overline{V_{\mathrm{CTRL}}}$ vary with time.

The π-network attenuator configuration offers a higher attenuation range than using a single NMOS device but at the cost of a higher insertion loss and a lower bandwidth. Transistor M_1 also serves as a load for the LO when the control impulse V_{CTRL} is low. This ensures an approximately constant loading impedance at the LO outputs regardless of the state of the impulse. The design of the variable attenuator involves several trade-offs, such as minimizing the on-state insertion loss, the off-state LO leakage and the pulse rise and fall times. Larger devices tend to reduce the insertion loss and increase the attenuation range; however, the increased parasitic capacitance adversely affects the bandwidth. In this design, on-chip spiral inductors are connected in series (series-peaking) as shown in Fig. 1 to absorb the transistors' parasitic capacitances and increase the bandwidth. The ac voltage gain $|A_V|$ of the attenuator has been simulated and plotted in Fig. 8. The minimum loss at the maximum gate voltage of $V_{\mathrm{CTRL}} = V_{DD} = 1.4$ V is about 4.0 dB. It is also evident that the maximum attenuation achieved at the center frequency of 24.0 GHz is 41 dB, giving an attenuation range of more than 30 dB. Note that 30 dB of attenuation range is sufficient since the LO can be switched off shortly after the pulse to mitigate LO leakage. Furthermore, the transmission in the on state remains quite flat, with less than 2.8 dB deviation over the 22–29 GHz UWB bandwidth.

III. Measurement and Simulation Results

A. Pulsed Quadrature Oscillator

The pulsed quadrature oscillator was first fabricated and characterized separately in 0.13 μm CMOS. A photograph of the

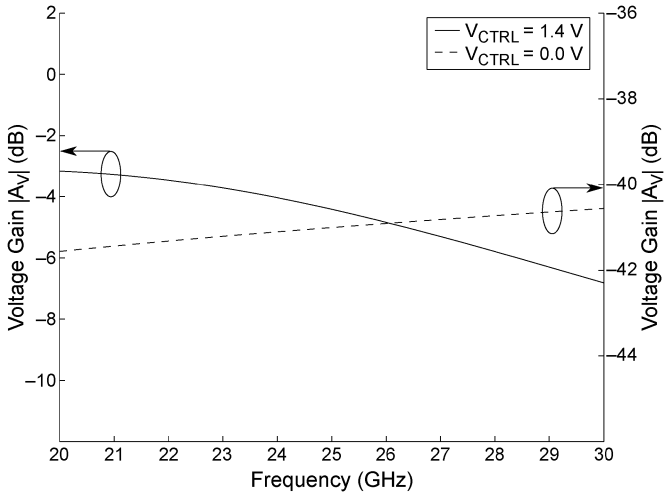

Fig. 8. Simulated voltage gain $|A_V|$ of the variable attenuator in the on-state ($V_{\mathrm{CTRL}} = 1.4$ V) and off-state ($V_{\mathrm{CTRL}} = 0.0$ V).

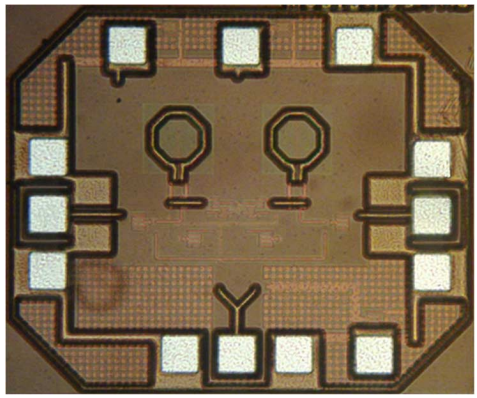

Fig. 9. Photograph of quadrature pulsed oscillator IC.

IC is shown in Fig. 9. It occupies a die area of 0.54 mm^2 including bonding pads, decoupling capacitors and the chip guard ring (plus chamfer regions), while the core circuit area is 0.17 mm^2.

The pulsed oscillator IC was measured directly on-wafer using 40 GHz coplanar waveguide (CPW) probes and dc probes. The Agilent 50 GHz spectrum analyzer (E4448A) was used to examine the output power spectrum and phase noise. Fig. 10 shows the measured output power spectrum when the quadrature oscillator is in free running mode, i.e., the input clock is held at logic high ($V_{DD} = 1.4$ V). The spectrum plot is centered at 23.9 GHz and covers a span of 500 MHz. It is clear that the free-running output power level is about -4.5 dBm at a frequency of 23.9 GHz. The phase noise of the free-running oscillations was measured and is plotted in Fig. 11 against the simulated phase noise. It is apparent that there is good agreement between measurement and simulation, and that a relatively low phase noise of -100 dBc/Hz is achieved at 1 MHz offset. The oscillation frequency can be tuned using the body biasing voltage V_B of the PMOS devices $M_{P1} - M_{P4}$ (Fig. 3), and Fig. 12 shows the measured oscillation frequency and output power level with different values of V_B. The results indicate that the tuning range is about 600 MHz, over which the output power varies by less than ± 1.5 dB.

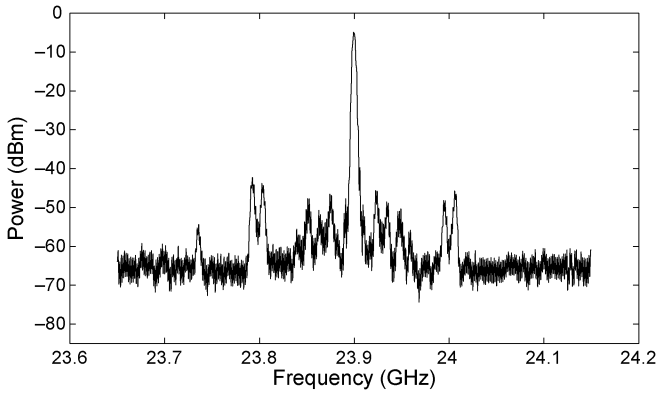

Fig. 10. Measured free-running output spectrum over a span of 500 MHz centered at 23.9 GHz.

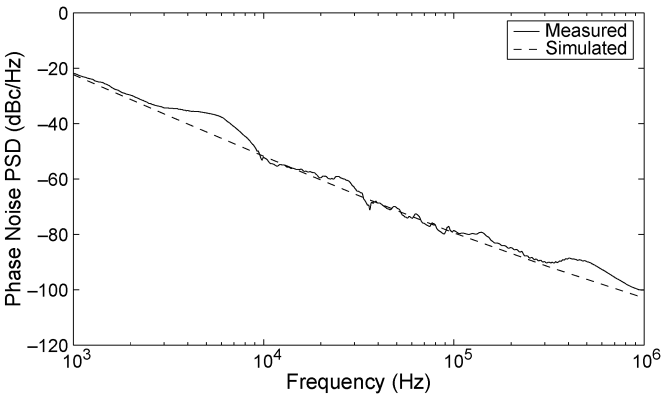

Fig. 11. Measured and simulated free-running output phase noise PSD from 1 kHz to 1 MHz.

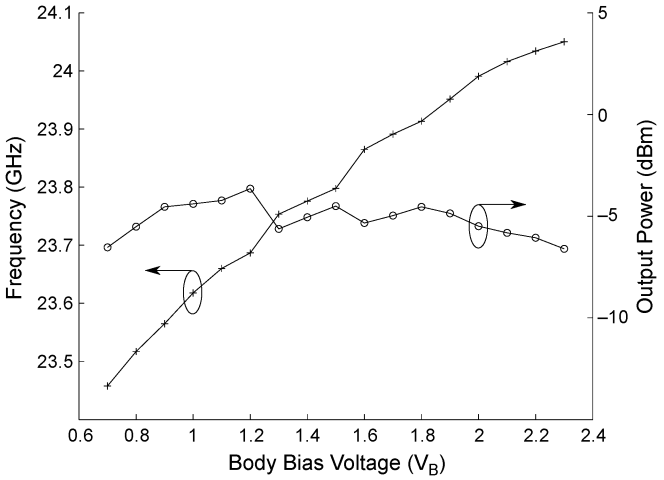

Fig. 12. Measured oscillation frequency and output power with different values of V_B.

The pulsed output power spectrum was also measured directly using a spectrum analyzer over a span of 8 GHz and is plotted in Fig. 13(a). The input clock is a periodic sinusoidal signal which is readily converted on-chip into a digital square wave using the edge sharpening inverters (Fig. 1). The clock frequency was set to about 500 MHz (508 MHz) for this measurement. The power spectrum exhibits peaks at multiples of the PRF since the output is a periodic (unmodulated) extension of the pulses. It is also apparent that the generated harmonic components are coherent and well-defined. Fig. 13(b) shows the

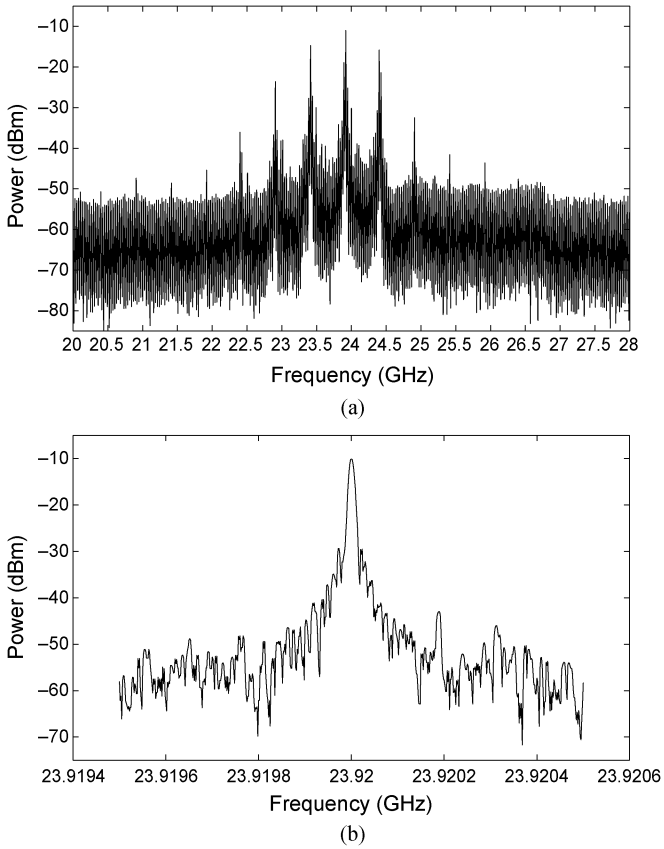

Fig. 13. Measured pulsed output spectrum at 24 GHz: (a) 8 GHz span and (b) 1 MHz span.

generated peak at 23.92 GHz in more detail over a span of only 1 MHz, clearly showing stable and locked operation.

Fig. 14 shows the measured phase noise of the generated pulsed output at 23.92 GHz. The measured phase noise of the clock reference and that of the free-running output shown in Fig. 11 are also included in Fig. 14 for comparison. As depicted in Fig. 14, the output phase noise matches that of the clock reference but is approximately 33 dB higher. This corresponds to the frequency ratio between the output and the clock reference since $20\log(23.92/0.508) = 33$ dB. Fig. 14 verifies that the 24-GHz pulsed oscillator is phase locked to the 500 MHz clock reference, achieving a relatively low phase noise of -62 dBc/Hz at 100 Hz, -70 dBc/Hz at 1 kHz and -65 dBc/Hz at 10 kHz. This amounts to a low integrated rms jitter of 720 fs from 100 Hz to 1 MHz.

The locking bandwidth of the oscillator was verified in both continuous and pulsed operation. In continuous operation, the input clock is held at logic high ($V_{DD} = 1.4$ V) and a 24 GHz sinusoidal signal is added using a bias-T for injection locking. The locking bandwidth f_L of the oscillator can be characterized by the well-known "Adler" formula given by

$$f_L = \frac{f_0}{Q}\sqrt{\frac{P_{\text{inj}}}{P_0}} \tag{5}$$

where f_0 is the free-running oscillator frequency, P_{inj} is the injected power level, P_0 is the oscillator output power level, and Q is the quality factor of the LC tank. Thus, the locking bandwidth f_L can be controlled by the injected-to-output power ratio

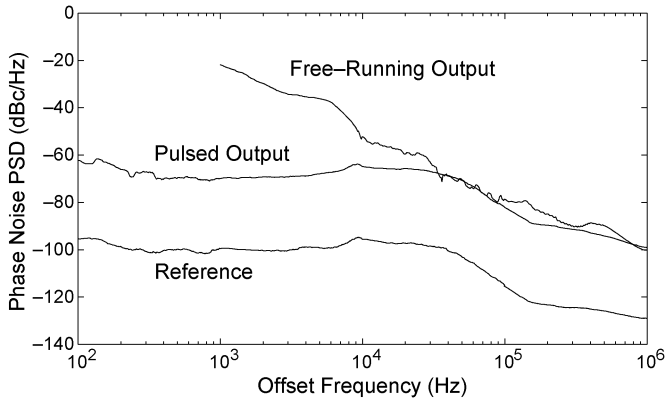

Fig. 14. Measured phase noise of pulsed output at 24 GHz.

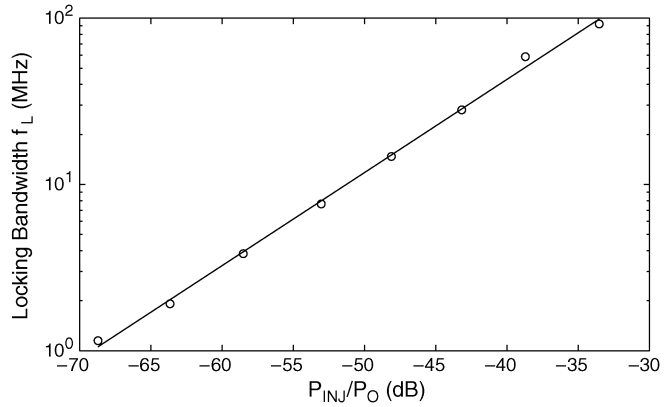

Fig. 15. Measured locking bandwidth for different levels of injected power $P_{\rm inj}$.

$P_{\rm inj}/P_0$. Fig. 15 shows the measured locking bandwidth for different injected power levels. It is clear that the locking bandwidth varies with the injected power according to (5), and that a locking bandwidth of 100 MHz is achieved at a low injected power level ($P_{\rm inj}/P_0 \approx -33$ dB). In pulsed operation, the oscillator output voltage amplitude and power level P_0 at startup are small compared to those in steady state. The current impulse $I_{\rm inj}$ injected at startup can also have a relatively large frequency component at 24 GHz as shown in Section II-A. Therefore a higher injected-to-output power ratio $P_{\rm inj}/P_0$ can be achieved for a wider locking bandwidth. The locking bandwidth was measured in pulsed operation and it was found to exceed 11 MHz around the 500 MHz input clock frequency. This translates to a locking bandwidth of more than 500 MHz at the output frequency of 23.9 GHz, thus ensuring phase-coherent pulsed operation.

The oscillator center frequency may drift due to changes in process, supply voltage and temperature (PVT). Simulations of the center frequency as a function of PVT variations are shown in Fig. 16. Corner simulation is performed in three modes (SS, TT, FF) to capture variations in process at the nominal supply voltage of 1.4 V and temperature of 25 °C. From Fig. 16(a), the oscillator frequency varies by about $\pm 1.6\%$ due to the process. Meanwhile, as the temperature changes from 0 °C to 75 °C in typical process conditions and at the nominal supply voltage, the oscillation frequency shows a variation of less than $\pm 0.75\%$ [Fig. 16(b)]. In addition, the oscillation frequency changes by

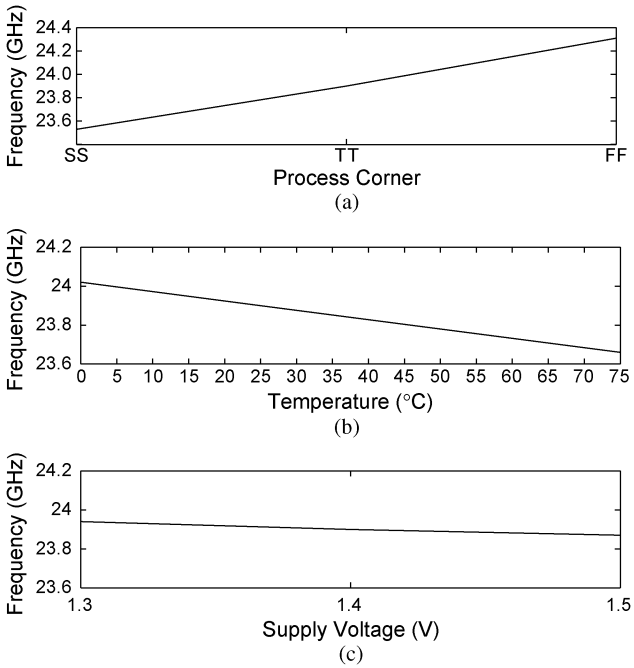

Fig. 16. Variations of the pulse center frequency with: (a) process, (b) temperature, and (c) supply voltage.

only $\pm 0.15\%$ [Fig. 16(c)] as the power supply voltage changes by ± 0.1 V at nominal process and temperature. These variations should be tolerable, since they are relatively small compared to the pulse frequency bandwidth of more than 2.7 GHz or 11%. The integrated power lost into adjacent channels, over a 2.7 GHz bandwidth would be relatively small and the receiver would still be able to detect the pulse to a certain extent. Furthermore, the oscillator frequency tuning range of 600 MHz and the available locking bandwidth of more than 500 MHz are sufficient to account for the PVT variations.

B. Quadrature Pulse Generator

The complete quadrature pulse generator was also fabricated in 0.13 μm CMOS and a photograph of the IC is shown in Fig. 17. It occupies a die area of 0.94 mm^2 including bonding pads, decoupling capacitors and the chip guard ring (plus chamfer regions), while the core circuit area is 0.41 mm^2. The circuit consumes less than 2.2 mW of average power ($P_{\rm AVG}$) at a PRF of 50 MHz. The power consumption increases with the PRF, reaching 14.8 mW at the maximum PRF of 600 MHz. This gives an energy consumption E_p of less than 11.0 pJ and 6.2 pJ at 50 MHz and 600 MHz PRF respectively for each of the four differential quadrature pulses. The energy consumption E_p is given by:

$$E_p = \frac{P_{\rm AVG} \times PRI}{4} = \frac{P_{\rm AVG}}{PRF \times 4} \tag{6}$$

where PRI is the pulse repetition time.

The UWB pulse generator IC was also measured directly on-wafer and a 60 GHz Tektronix Digital Serial Analyzer (DSA) was used to observe the pulses in the time domain. The input clock is a periodic sinusoidal signal which is readily converted on-chip into a digital square wave using the edge sharpening

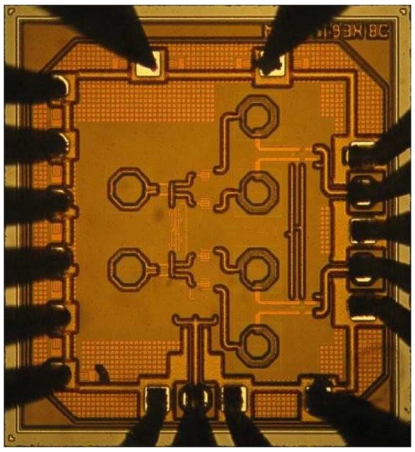

Fig. 17. Photograph of quadrature UWB pulse generator IC.

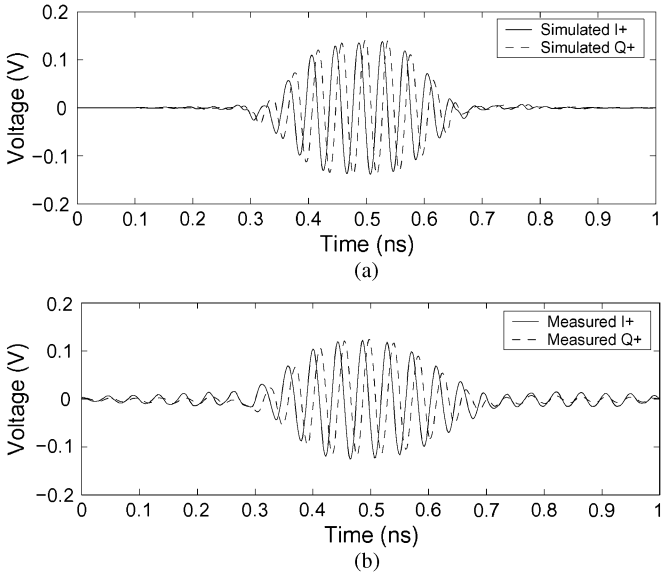

Fig. 18. Output UWB waveforms: (a) simulated and (b) measured.

inverters (Fig. 1). Fig. 18 shows a comparison between a simulated output signal and the DSA's measurement result. Both simulation and measurements have the same bias conditions, and there is good agreement between the simulated and measured waveforms. The measured pulses have a peak-to-peak voltage amplitude of 240 mV and a peak power level of -5.4 dBm, with good symmetry about the 0 V (ground) level $(V_{pk+} + V_{pk-})/(V_{pk+} - V_{pk-}) \approx 2\%$. The ringing level is also about -24.0 dB, which is somewhat higher than simulated, most probably due to unmodeled substrate coupling and inductive parasitics. The pulse time duration can be tuned over a wide range using the control voltages V_{WIDTH} and V_{SLOPE} in the glitch generator and Fig. 19 shows the measured pulses with time durations of 375 ps, 525 ps, and 650 ps. Moreover, the phase difference between the $I+$ and $Q+$ outputs is about $90 \pm 3.0°$. It should be noted that the DSA is an equivalent time sampling oscilloscope and not a real-time oscillocope, sampling the signal only once per trigger event. The DSA is thus triggered using the input clock for this measurement. Since 24 GHz cycles with a time period of around 40 ps are clearly visible, the generated

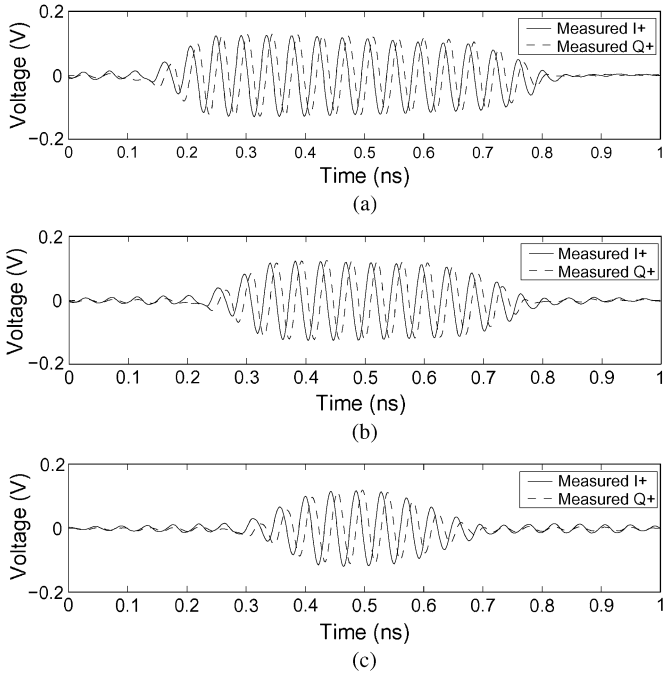

Fig. 19. Measured UWB waveforms with different time durations: (a) long (650 ps), (b) moderate (525 ps), and (c) short (375 ps).

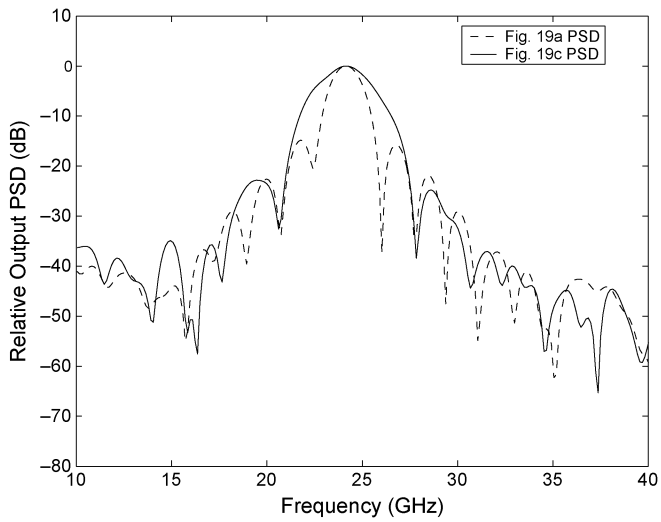

Fig. 20. Calculated normalized PSD of the measured output UWB signals.

oscillations are indeed coherent with the input clock, and thus pulse-to-pulse coherency is maintained.

The normalized power spectral density (PSD) of the measured signals shown in Fig. 19(a) and Fig. 19(c) was calculated and is illustrated in Fig. 20. It is apparent that the measured -10 dB bandwidth varies from about 2.7 GHz to 4.9 GHz and is centered at 23.9 GHz which corresponds to the LO signal frequency. The spectra are also free from spikes or spectral lines that occur due to LO leakage in typical pulse generators. Furthermore the spectrum roll-off can be quite sharp with more than 23 dB of out-of-band rejection relative to the peak power level for the pulse in Fig. 19(c).

Table I summarizes the circuit's characteristics in comparison with other work [8], [11], [18], [25]–[27]. The proposed pulse generator offers quadrature tunable outputs with comparable or

TABLE I
SUMMARY OF UWB PULSE GENERATOR CHARACTERISTICS

Characteristic	**This work**	[11]	[8]	[27]	[18]	[25]	[26]
Technology	**0.13 μm** CMOS	0.13 μm SiGe	0.18 μm CMOS	0.13 μm InP-HEMT	90 nm CMOS	GaAs HBT	GaAs HBT
Circuit Area (mm^2)	**0.41**	–	–	2.55	0.0014 [1]	1.17	1.0
Power (mW)	**14.8**	14.5 [2]	42	620	1.4	55	–
PRF (MHz)	**600**	10	–	–	500	62.5	10
Energy	**6.2 pJ/pulse**	–	–	–	2.8 pJ/pulse	–	–
Pulse Amplitude	**240 mV**	630 mV	80 mV [3]	800 mV	71 mV	1.4 V	600 mV
Pulse Width	**$\geq$ 375 ps**	1.1 ns	250 ps	$<$ 500 ps	552 ps	1.0 ns	900 ps
Carrier Frequency (GHz)	**23.9**	24.125	26.5	26.5	25.5	24.31	26.5
Phase Noise (dBc/Hz)	**-70 at 1 kHz** **-100 at 1 MHz**	-56 at 1 kHz -104.3 at 1 MHz	-57 at 10 kHz -107 at 1 MHz	–	–	-102.5 at 100 kHz -120.83 at 1 MHz	–

better phase noise at a low energy consumption of 6.2 pJ/pulse. It is also more energy efficient than most of the other designs if the energy consumption is normalized with respect to the output peak-to-peak voltage. Furthermore, the proposed circuit has a relatively small area compared to the other work.

IV. CONCLUSION

A new quadrature tunable pulse generator has been developed in 0.13 μm CMOS for 22–29 GHz UWB applications. A quadrature LC oscillator is quickly switched on and off for the pulse duration, and the amplitude envelope is shaped using a variable passive CMOS attenuator. By switching on one side of each differential oscillator just before the other, a current impulse is injected with a short time duration and large harmonic components out to 24 GHz, creating a large initial condition for fast startup and setting the initial phase of the oscillations for high pulse-to-pulse coherence. The measured output phase noise thus matches that of the clock signal, yielding a relatively low phase noise of -70 dBc/Hz at 1 kHz offset, and -100 dBc/Hz at 1 MHz offset. This amounts to a low integrated rms jitter from 100 Hz to 1 MHz of less than 720 fs. The attenuator is controlled with an impulse which is created by a digital, tunable glitch generator (CMOS NAND gate). Several UWB pulses were measured and demonstrated, with the pulse time duration and -10 dB bandwidth varying over a range of 375–650 ps and 2.7–4.9 GHz respectively. The entire circuit operates in switched-mode with a low average power consumption of less than 2.2 mW and 14.8 mW at 50 MHz and 600 MHz PRFs, or below 11 pJ for each of the four differential quadrature pulses. It occupies a total area of 0.94 mm^2 including bonding pads and decoupling capacitors, and the active circuit area is only 0.41 mm^2.

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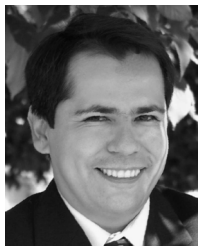

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