A 12 GHz-Bandwidth CMOS Mixer With Variable Conversion Gain Capability

Jiangtao Xu, *Student Member, IEEE*, Carlos E. Saavedra, *Senior Member, IEEE*, and Guican Chen

***Abstract*—A broadband downconverter mixer using an operational transconductance amplifier (OTA) in the RF transconductor stage is presented in this paper. By changing the OTA's transconductance through a dc control voltage, the mixer's conversion gain is varied. Experimental results show that the mixer's conversion gain can vary from 17 dB down to 1.2 dB over a 12 GHz bandwidth. The maximum $\mathrm{IP}_{1\,\mathrm{dB}}$ of the mixer is −3.7 dBm and its maximum IIP3 is +8.6 dBm. Meanwhile, the maximum $\mathrm{OP}_{1\,\mathrm{dB}}$ is +7 dBm and the maximum OIP3 is +21 dBm. The circuit consumes a maximum of 5.9 mW of power from a 1.2 V supply. The chip occupies an area of 0.105 mm^2 excluding bonding pads.**

***Index Terms*—Broadband, CMOS, high-linearity, mixer, operational transconductance amplifier (OTA), RFIC, variable conversion gain.**

I. Introduction

In microwave transceiver RFICs with gain-control capability, unifying the frequency mixing and gain control functions into a single circuit can lead to savings in chip area and reduce overall system complexity. The resulting circuit component is a mixer with variable conversion gain and a number of these type of mixers have been reported in the literature, both downconverters [1]–[4] and upconverters [5].

In this paper, a very wideband operational transconductance amplifier (OTA) is used together with a Gilbert-type switching core and an IF load to implement a new variable conversion gain mixer circuit. The mixer's conversion gain can be varied from 17 dB and down to 1.2 dB while maintaining a relatively high $\mathrm{IP}_{1\,\mathrm{dB}}$ and IIP_3 as its gain changes. The OTA circuit is used as the RF transconductor for the mixer and its dc bias current is decoupled from that of the switching core and load. This arrangement, in conjunction with the folded mixer topology, helps to reduce the dc power consumption of the chip.

II. Circuit Design

A system-level schematic of the proposed mixer is shown in Fig. 1. A wideband OTA is used to convert the RF input signal into a pair of differential currents that are subsequently fed to the switching core. The OTA's transconductance can be changed over a large range through the control voltage, V_{CTL}, enabling the mixer to have a variable conversion gain. An inductive impedance, Z_{pk}, between the OTA and the switching core is used for shunt-peaking in order to increase the operating bandwidth of the mixer. The mixer's load is a network of pMOS transistors so that together with the nMOS switching core the result is a folded mixer architecture which allows for a large conversion gain in the high-gain state while simultaneously keeping the dc power consumption low.

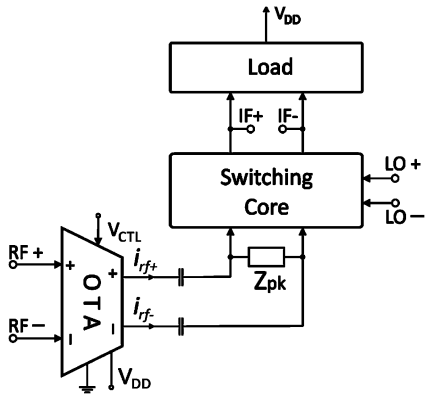

Fig. 1. System-level diagram of the proposed downconverter mixer.

The schematic of the OTA [6] used in this design is shown in Fig. 2. The input transconductor stage is formed by the transistors M_1 and M_2 operating in the triode region. The regulated cascode stage M_3 and M_4 and the cross-coupled capacitors C_5 and C_6 form an interlocking mechanism to stabilize the voltages at the drains of M_1 and M_2 and thus enhance its linearity [7], [8]. The transconductance, G_m, of the OTA can be changed through the gate bias voltage of transistors M_3 and M_4, and is labeled V_{CTL}. For more details about this OTA, see [6], [7] as well as [8], which contains Monte-Carlo simulations regarding the impact of process variations on G_m.

The mixer switching core and the active IF load network are depicted in Fig. 3. The main signal path in the load network is through transistors M_{11} and M_{12} while devices M_{13} and M_{14} are used as ON/OFF switches to maximize the mixer's conversion gain range. When devices M_{13} and M_{14} are switched OFF, the active load impedance is at its largest value, which places the mixer in the high-gain mode. Conversely, when those two devices are switched ON, resistors $\mathrm{R}_{11}/\mathrm{R}_{12}$ are now in parallel with transistors $\mathrm{M}_{11}/\mathrm{M}_{12}$ which reduces the active load impedance and consequently the mixer operates in the low-gain mode. In Fig. 3, resistors R_9, R_{10}, R_{13} and R_{14} have large values and are used for biasing, while R_7 and R_8 have small values to flatten the frequency response.

Manuscript received June 10, 2010; revised October 13, 2010 and May 02, 2011; accepted July 21, 2011. Date of publication August 18, 2011; date of current version October 07, 2011. This work was supported, in part, by NSERC, CMC Microsystems, Canada, and a aChina Scholarship Council Award.

J. Xu is with the School of Electronics and Information, Xi'an Jiaotong University, Xi'an, 710049, China and also with Queen's University, Kingston, ON, K7L 3N6 Canada.

C. E. Saavedra is with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, K7L 3N6, Canada (e-mail: saavedra@queensu.ca).

G. Chen is with the School of Electronics and Information, Xi'an Jiaotong University, Xi'an 710049, China.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LMWC.2011.2163387

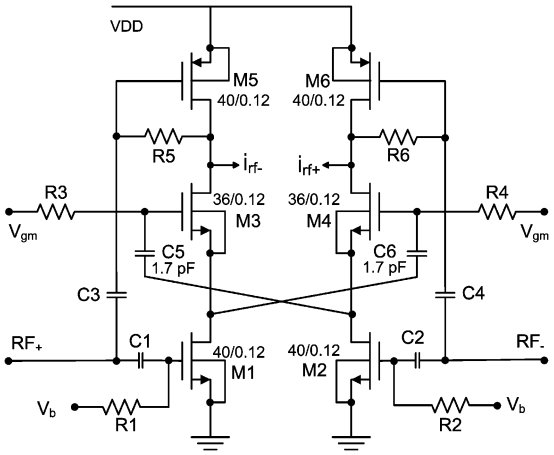

Fig. 2. The wideband OTA with variable transconductance.

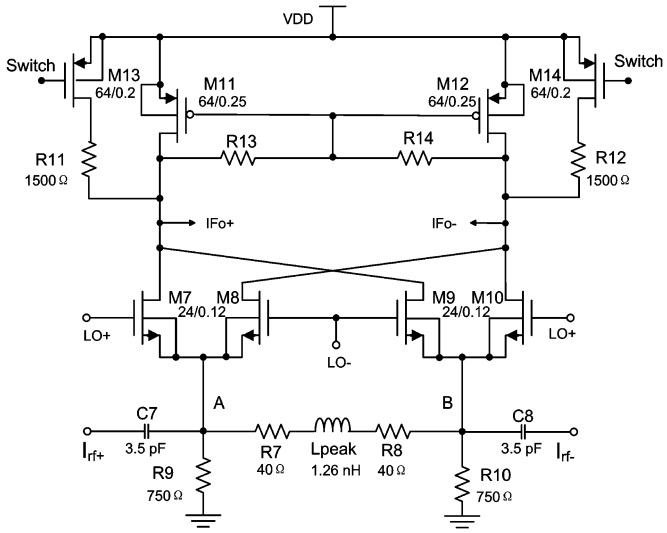

Fig. 3. The mixing core and the active load network.

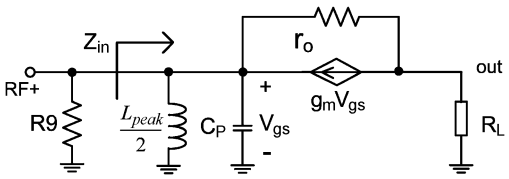

Fig. 4. Half-equivalent circuit incorporating the shunt-peaking inductance.

Inductor L_{peak} in Fig. 3 is employed as a shunt-peaking inductance to expand the frequency response of the mixer. Fig. 4 shows the half-circuit equivalent model looking into the switching core. C_p represents the output capacitance of the OTA plus the source parasitic capacitance of devices $\mathrm{M}_7-\mathrm{M}_{10}$. In addition, g_m and r_o are the transconductance and output resistance of the switching core, and R_L is the load impedance. The input impedance, Z_{in}, in Fig. 4 can be written as

$$Z_{in} = \frac{1}{K}\frac{s^2 L_{peak}C_p + 1}{s^2 L_{peak}C_p + sC_p/K + 1} \tag{1}$$

where $K = (g_m + (1/r_0))/(1 + (R_L/r_0))$. The introduction of L_{peak} results in a notch at $\omega = 1/\sqrt{L_{peak}C_p}$. This notch is designed at the high frequency end of the bandwidth, i.e. around 12 GHz, so Z_{in} exhibits a smaller load impedance to the OTA at higher frequencies, which means that more RF currents will be drawn out of the OTA, thereby increasing the conversion gain of the mixer at the high-frequency end.

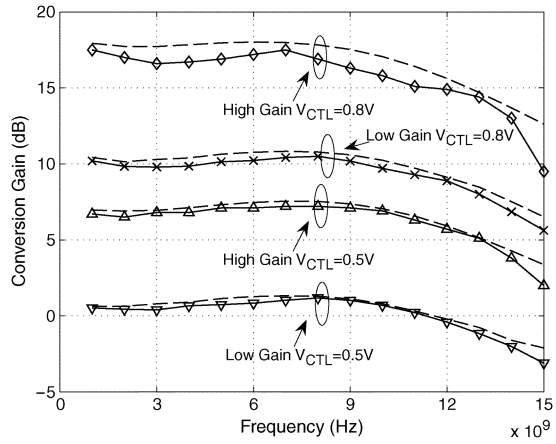

Fig. 5. Measured (solid lines) and simulated (dotted) conversion gain versus frequency.

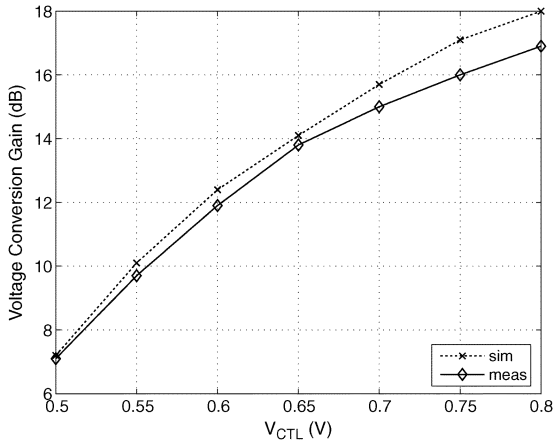

Fig. 6. Conversion gain versus V_{CTL} at 5 GHz (high-gain mode).

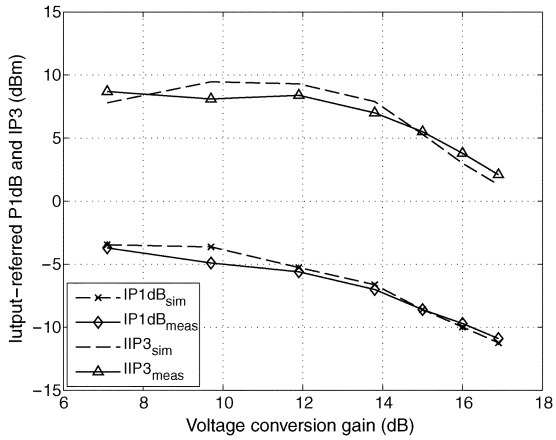

Fig. 7. $\mathrm{IP}_{1\,\mathrm{dB}}$ and IIP_3 versus conversion gain at 5 GHz (high-gain mode).

III. Experimental Results

The mixer was fabricated in a standard 130 nm CMOS process, and the circuit core occupies an area of 0.105 mm^2. The chip was biased from a 1.2 V supply and it consumes a maximum power of 5.9 mW when the mixer is in the highest gain setting and a minimum of 1.8 mW in the lowest gain setting.

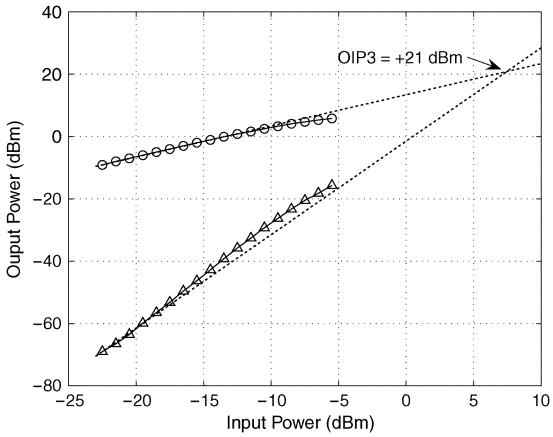

Fig. 8. Representative two-tone test at $V_{CTL} = 0.65$ V (high-gain mode).

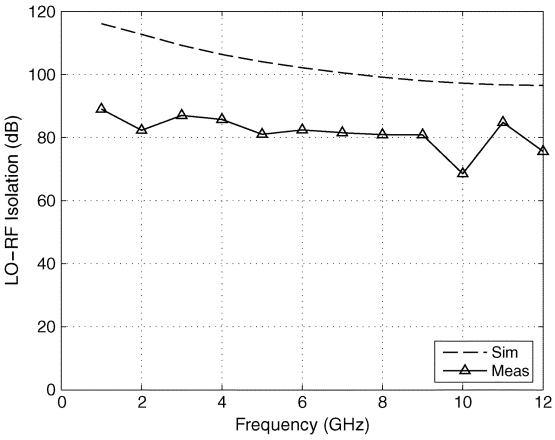

Fig. 9. Measured LO-to-RF port isolation at 5 GHz and a typical gain setting.

TABLE I
COMPARISON BETWEEN VARIABLE CONVERSION GAIN MIXERS

Ref.	Freq. (GHz)	Gain Range (dB)	IP_{1dB} (dBm)	IIP3 (dBm)	Min. NF (dB)	P_{DC} (mW)
This	**1−12**	**+1.2 to +17**	**−3.7**	**+8.6**	**11**	**5.9**
[1]	2−10	+9 to +24	−4	+3.5	8	18
[2]	1.6	−50 to 0	−2	n/a	n/a	7.6
[3]	28−37	−21.2 to −11.9	n/a	n/a	n/a	0
[4]	5.25	−28 to +6.2	−16	−3.9	18.8	7.2

Using an IF frequency of 110 MHz the frequency response of the mixer was measured at different gain levels as shown in Fig. 5. With the mixer set to the high-gain mode, the maximum conversion gain was measured at 17 dB when the OTA's control voltage, V_{CTL}, equals 0.8 V. The gain can be reduced to 7 dB as V_{CTL} is lowered to 0.5 V. When the mixer is set to the low-gain mode, the gain ranges from 10.5 dB to an absolute minimum of 1.2 dB, resulting in a gain overlap range of 3.5 dB between the low and high-gain modes. As shown in Fig. 5, the mixer has a large 3 dB bandwidth of 12 GHz. A graph of conversion gain versus control voltage in the high-gain mode at a representative frequency of 5 GHz is shown in Fig. 6.

Several two-tone tests were carried out to evaluate the mixer's power performance at different conversion gain levels. The tests were done at a mid-band frequency of 5 GHz in the high gain mode and the tones were spaced 1 MHz apart. The results of those tests are shown in Fig. 7. The maximum $IP_{1\,dB}$ is −3.7 dBm and the maximum IIP3 is +8.6 dBm. The corresponding maxima for the $OP_{1\,dB}$ and OIP3 are +7 dBm and +21 dBm, respectively. A representative two-tone test result graph when V_{CTL} was set to 0.65 V is shown in Fig. 8.

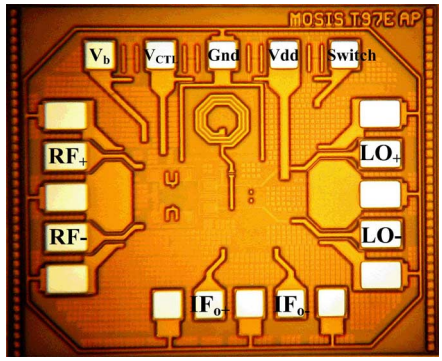

Fig. 10. Microphotograph of the proposed mixer.

The measured isolation between LO and RF ports is shown in Fig. 9 and it is higher than 70 dB over the entire 12 GHz band. The double sideband noise figure of the mixer was measured, and it has a minimum value of 11 dB when the conversion gain is set to 17 dB while a maximum value of 19 dB when the conversion gain is set to 7 dB.

A performance summary and comparison table with other variable-gain downconverter mixers is presented in Table I. A microphotograph of the chip is shown in Fig. 10.

IV. CONCLUSION

A new concept for a mixer with variable conversion gain has been demonstrated. The circuit achieves a wide 3 dB bandwidth of over 12 GHz because it uses a very high-speed OTA in the RF transconductance stage. The mixer has high linearity performance and its gain can vary over a wide range.

REFERENCES

[1] M. Wang and C. E. Saavedra, "Reconfigurable broadband mixer with variable conversion gain," in *IEEE MTT-S Int. Dig.*, Jun. 2011, pp. 1–4.
[2] C. W. Ryu, C. S. Cho, J. Lee, and J. Kim, "A low power 45 dB dynamic-range variable gain mixer in 0.18 μm CMOS," in *IEEE MTT-S Int. Dig.*, 2009, vol. 7–12, pp. 585–588.
[3] C.-H. Lin, J.-C. Chiu, C.-M. Lin, Y.-A. Lai, and Y.-H. Wang, "A variable conversion gain star mixer for Ka-band applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 11, pp. 802–804, Nov. 2007.
[4] J.-Y. Hsieh and S.-Y. Lee, "Theoretical analysis and implementation of a variable gain even harmonic mixer," in *Proc. Int. Symp. VLSI Design, Autom. Test*, 2007, vol. 25–27, pp. 1–4.
[5] K. Kobayashi, A. Gutierrez-Aitken, J. Cowles, B. Tang, R. Desrosiers, V. Medvedev, L. Tran, T. Block, A. Oki, and D. Streit, "15 dB gain, DC-20 GHz InP HBT balanced analog mixer and variable gain amplifier with 27 dB of dynamic range," in *Proc. IEEE Radio Freq. Integr. Circuits (RFIC) Symp.*, 1999, pp. 105–108.
[6] J. Xu, C. E. Saavedra, and G. Chen, "Wideband microwave OTA with tunable transconductance using feedforward regulation and an active inductor load," in *Proc. 8th IEEE Int. NEWCAS Conf. (NEWCAS)*, , 2010, pp. 93–96.
[7] Y. Zheng and C. E. Saavedra, "Full 360 ° vector-sum phase-shifter for microwave system applications," *IEEE Trans.Circuits Syst. I,*, vol. 57, no. 4, pp. 752–758, Apr. 2010.
[8] Y. Zheng and C. E. Saavedra, "Feedforward-regulated cascode OTA for gigahertz applications," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 11, pp. 3373–3382, Dec. 2008.