Chapter 5

Analog Frequency Multiplier Design Techniques and Applications

Carlos E. Saavedra

Department of Electrical and Computer Engineering

Queen's University, Kingston, Ontario, Canada

5.1 Introduction

Generating periodic waveforms with high spectral purity becomes progressively difficult as the signal frequency increases. Certain applications need exceptionally pure signals and often the best way to generate them is by using a very stable, low-frequency, oscillator followed by a frequency multiplier circuit which upconverts the signal to the desired frequency band. Some of these applications include the clocks needed to synchronize the circuitry gates in modern microprocessor integrated circuits. Another application is in high-performance broadband communications, where the bit error ratio of the system is related to the noise performance

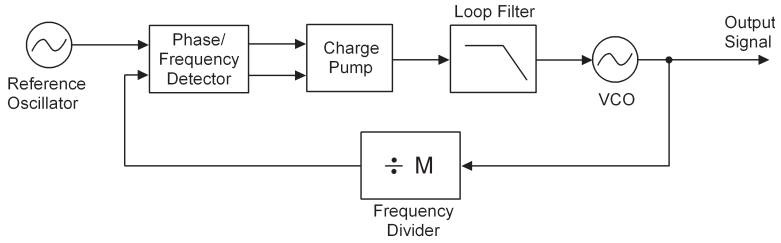

Figure 5.1: Basic frequency synthesizer architecture

of the electronic and optical components, specially the local oscillators. This chapter begins with a brief review of the basic principles and ideas behind frequency multipliers and this is followed by a more extensive discussion of recent advances in multiplier design.

5.2 Multipliers for Very High-Speed Computing and Communications Systems

The generation of periodic signals, or clocks, is of fundamental importance in any computing system. Since clocks are used for time-keeping purposes they must be exceptionally stable over long periods of time and also over temperature. Temperature-compensated quartz oscillators (TCXO's), for example, have a phase-noise of around -150 dBc/Hz at a 10 kHz offset from a 10 MHz carrier. This level of frequency stability is highly desirable in microprocessors and a variety of other systems in order to minimize bit errors.

Modern computing systems have clock frequencies in the gigahertz range, yet quartz-based oscillators have an upper frequency limit of between 100 to 200 MHz even when using the crystal's higher-order overtones. At the present time, the most common approach [1] [2] to generate very stable waveforms at RF frequencies is to use a phase-lock loop (PLL) that uses a crystal oscillator as the reference oscillator as shown in Fig. 5.1. In this frequency synthesizer, the voltage-controlled oscillator (VCO) runs at the desired RF frequency, f_{out}, and the frequency divider in the feedback path brings the RF signal frequency down to the

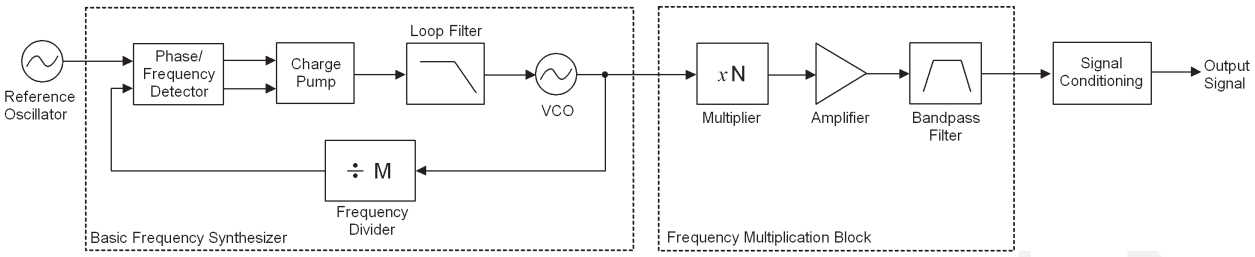

Figure 5.2: Synthesizer for very high frequencies

range of the reference crystal oscillator, f_{ref}. The feedback mechanism forces the VCO's output frequency to obey the condition, $f_{out} = Mf_{ref}$, and it simultaneously stabilizes the VCO. Recent work [3] has shown that oscillators using film bulk-acoustic wave resonators (FBAR's) can have a phase-noise of -125 dBc/Hz at 10 kHz from a 1.5 GHz carrier, which is very promising, and it is possible that in the not too distant future FBAR oscillators will start to be used in commercial RF applications.

To generate very high frequency local oscillator signals for millimeter-wave transceivers, for instance, it is possible to introduce a frequency multiplication block after the PLL [4]. An example of such a synthesizer is depicted in Fig. 5.2, where the multiplier circuit yield the output frequency $f_{out} = MNf_{ref}$. If a passive multiplier circuit is used then the amplifier will compensate for the conversion loss of the multiplier. Since the signal that emerges from the bandpass filter will likely be sinusoidal in nature, then signal conditioning circuitry will be necessary to properly shape the output waveform if the synthesizer is to be used for clocking purposes in very high-speed digital or mixed-signal custom integrated circuits.

5.3 Noise Concepts in Frequency Multipliers

In the frequency domain, the output signal of an oscillator can be visualized as a spectral line that is randomly fluctuating around a center frequency point, ω_o, due to noise processes in the system. Therefore, the instantaneous frequency of the oscillator can be written as,

$\omega(t) = \omega_o + \delta\omega(t)$ where $\delta\omega(t)$ represents the frequency fluctuation. Since frequency is the derivative of phase with respect to time, it follows that $\delta\omega(t) = d\phi(t)/dt$ and this leads to,

$$\omega(t) = \omega_o + \frac{d\phi(t)}{dt} \tag{5.1}$$

Using Eqn. (5.1), the oscillator output signal in the time domain is modeled by the expression,

$$u(t) = A(t)\cos[\omega(t)t] = A(t)\cos\left[\omega_o t + \frac{d\phi(t)}{dt}t\right] \tag{5.2}$$

In the above equation, $A(t)$ represents AM noise, but oscillators running in steady-state generally have small amplitude variations and furthermore, these can be minimized by using a limiting amplifier if needed. Thus $A(t)$ will be set to the constant value, A_0 for the remainder of this discussion. Note that the term $(d\phi(t)/dt)t$ in Eqn. (5.2) has units of radians, and we will make the further substitution $\Delta\phi(t) \equiv (d\phi(t)/dt)t$ in this section. Using the simpler term $\Delta\phi(t)$ reinforces the notion that the frequency fluctuations of an oscillator are in essence phase fluctuations. When discussing oscillator phase-noise, the concept of the noise spectral density of the phase fluctuations is often invoked. In logarithmic terms, this spectral density is given by,

$$S_\phi(f_m) = 10\log\Delta\phi_{rms}^2 = 20\log\Delta\phi_{rms} \tag{5.3}$$

which has units of dBr/Hz, or decibels above one radian per one hertz of bandwidth. The frequency f_m in Eqn. (5.3) is the offset frequency from the center at which the phase noise is measured.

When the output of an oscillator is connected to a $\times n$ frequency multiplier, not only is the center frequency multiplied by n but the phase fluctuations are also multiplied by the same factor [5] [6], meaning that the spectral purity of the output signal is degraded relative to the input signal. If the input to the multiplier is given by Eqn. (5.2), then the output

signal at the desired upconverted frequency is,

$$v(t) = B_0 \cos\left[n\omega_o t + n\Delta\phi(t)\right] \tag{5.4}$$

Calculating the noise spectral density of the phase fluctuations of this signal with the aid of Eqn. (5.3), the following expression is easily obtained,

$$S_\phi^{(n)}(f_m) = 20\log(n\Delta\phi_{rms}) = 20\log n + 20\log\Delta\phi_{rms} \tag{5.5}$$

In practical terms, this expression says that if one measures the phase noise at the output of a frequency multiplier, that phase noise will be $20\log n$ worse than the phase noise of the input signal, where n is the multiplication factor. Note that phase noise is measured at the same offset frequency relative to the carrier in both instances and furthermore the $20\log n$ phase-noise degradation is a theoretical *minimum* because the expression does not include the internal noise of the multiplier circuit itself. A well-designed multiplier, however, can often achieve a phase-noise degradation that is not too much larger than the theoretical minimum.

5.4 Single-Transistor Frequency Multipliers

An active frequency multiplier can be implemented using a single transistor [7]. Either a field-effect transistor or a bipolar device can be used but here we will focus the discussion on FET devices since they are more commonly used. The basic topology of a FET multiplier is depicted in Fig. 5.3. The output coupling network can be either a filter or a simple arrangment of stubs whose purpose is to filter out the unwanted harmonics from the output spectrum and to isolate the desired tone. The input coupling network is mainly used for impedance matching purposes.

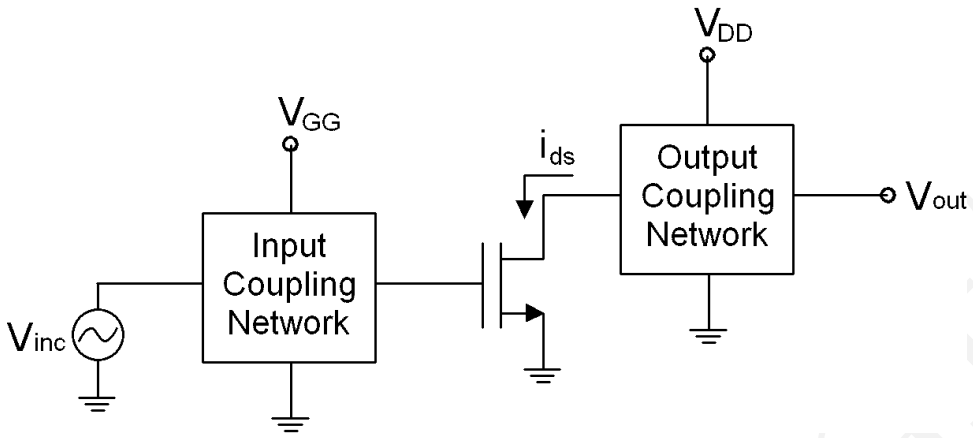

Figure 5.3: Single-FET frequency multiplier. After [7].

The dc gate bias of the device, V_{GG}, is chosen such that it is somewhat below the transistor threshold voltage, V_{tn}. When the incident RF signal, V_{inc}, is superimposed on V_{GG}, the voltage gate will rise above V_{tn} and the transistor will turn on for part of the wave cycle. In the time domain, the resulting drain current i_{ds} of the transistor will be a pulsed waveform with lots of harmonics,

$$i_{ds} = I_0 + \sum_{n=1}^{\infty} I_n \cos(n\omega_{in} t) \tag{5.6}$$

where ω_{in} is the incident frequency and the Fourier coefficients are given by [8],

$$I_n = I_{pk} \frac{4t_0}{\pi T} \left| \frac{\cos(n\pi t_0/T)}{1-(2nt_0/T)^2} \right| \tag{5.7}$$

In Eqn. 5.7, I_{pk} is the peak pulsed current, t_0 is the current pulse duration and T is the period of the input signal to be multiplied.

A graphical representation of the waveforms described in the previous paragraph using a 1 GHz input signal can be seen in the top row of Fig. 5.4. The dashed line in the graph on the left is the threshold voltage of the device, which is about 0.48 V for a 130 nm NMOS transistor and the spectral plot on the right show the amplitude of the harmonics of i_{ds} relative to the fundamental tone. We note that the strength of the second harmonic at 2

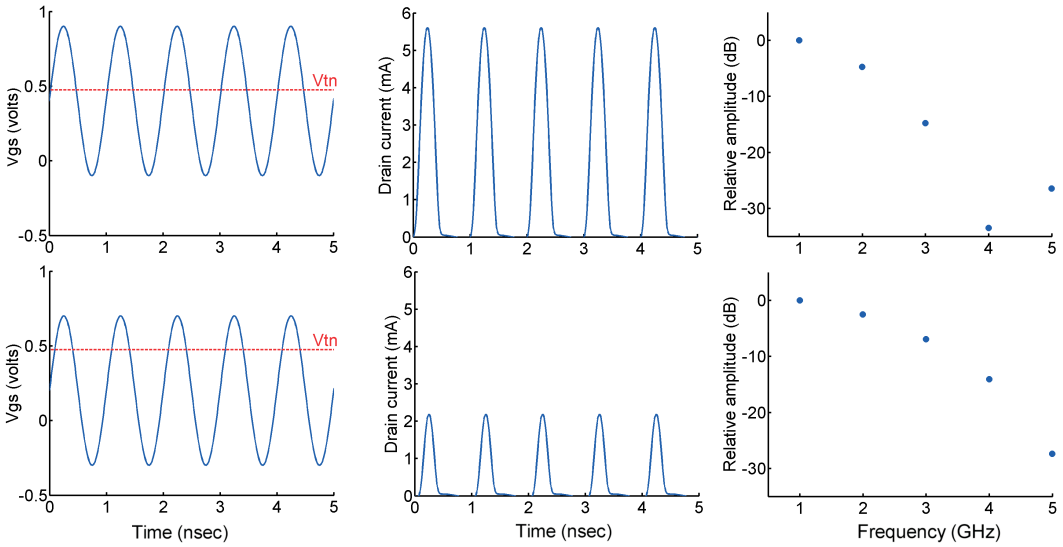

Figure 5.4: Representative voltage and current waveforms for the multiplier in Fig. 5.3

GHz is – 5 dB and for the third harmonic it is about – 15 dB relative to the fundamental, and therefore we see that the circuit in Fig. 5.3 can function quite well as a doubler circuit but not as well as a tripler.

One solution to get better results from this circuit in tripler mode is just to decrease the dc bias voltage at the gate. As the dc gate voltage is decreased, the duty cycle of the output current pulses will become shorter and the harmonic content of i_{ds} will become stronger. A graphical representation of this effect is shown in the plots in the bottom row of Fig. 5.4. Now the third harmonic is approximately – 7 dB relative to the fundamental, which represents an improvment of + 8 dB compared to what we had before. However, there is a cost associated with this simple approach: the absoulte output power levels of the harmonic signals are lower than before because peaks of the current pulses decreased from 5.6 mA to around 2.2 mA, as can be seen in the two middle plots in Fig. 5.4. The decrease in the output power levels translates into a higher conversion loss. Recently, new circuit concepts [9] [10] have appeared in frequency tripler design which overcome some of the conversion loss issues encountered with the single-FET approach of Fig. 5.3, and we will discuss them later in this

chapter.

While a single device can produce a double frequency quite easily, it also produces a strong fundamental tone that must be removed. The filters used to remove the fundamental and other unwanted harmonics naturally impose bandwidth restrictions on the useable frequency range of the multiplier. An interesting way to create a very broadband frequency doubler is to use traveling-wave techniques. The approach was inspired by the extensive literature that exists in the area of distributed amplifiers [11].

Fig. 5.5 shows two distritubed multiplier implementations using unbalanced and balanced RF inputs. The design in Fig. 5.5(a) was first described in [12] and it consists of two rows of FET's. In the top row the transistors are in a common-gate (CG) configuration with the RF input signal entering the devices at the source terminals. The gate bias voltage, V_{G1}, is such that the transistors are near pinchoff and hence they generate the second harmonic. The second harmonic emerging from the drains of the devices add constructively in the top transmission line as the wave travels in the forward path toward the output. There will also be an undesired fundamental tone traveling in the top transmission line which is in-phase with the RF input signal since the top row of devices are in CG mode.

The transistors in the lower row are in a common-source (CS) arrangement and therefore the fundamental tone travelling in the bottom transmission line will be out-of-phase with respect to the RF input signal. Fortunately, however, the second harmonic generated will be *in-phase* relative to the top row since doubling the frequency also doubles the phase and it does not matter if phase of the fundamental input was 0 or π. This is simply because if a signal of the type $\cos(\omega t + \pi)$ is fed to a doubler, the output at the second harmonic will be $\cos(2\omega t + 2\pi) = \cos(2\omega t)$, and the phase information of the fundamental tone is removed.

When the signals traveling in the top and bottom tranmission lines are added at the output node in Fig. 5.5(a), the tones at the second harmonic will experience constructive

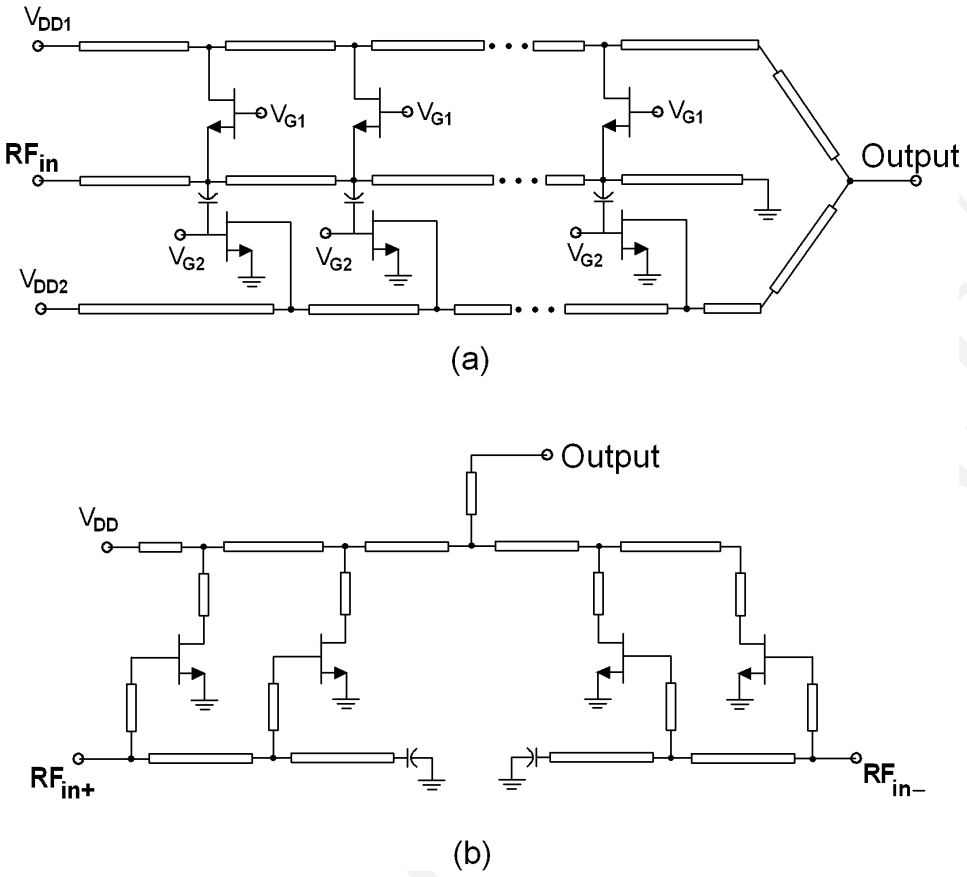

Figure 5.5: Broadband traveling-wave frequency doublers with (a) unbalanced input and (b) balanced input. After [12] and [13].

intereference while the fundamental tones will experience destructive interference. The result is a broadband doubler circuit that does not require output filtering of the fundamental tone. The results reported in [12] indicate that using an RF input power of +18 dBm will yield a fundamental supression of 16 dB and a conversion loss of 10 to 14 dB in the output frequency range of 10–18 GHz. The high RF input power needed is most likely the result of having to feed a large number of transistors from a single source.

The distributed multiplier shown in Fig. 5.5(b) is a more recent version [13] of the traveling-wave multiplier just described, but with the modification that the RF input signal is a differential waveform. As before, the second harmonic tones add constructively at the output node since the doubling process removes the phase information from the input signal,

and the fundamental tones interfere destructively at the output. A benefit of arranging all of the transistors in common-source mode in this circuit is that only two dc bias voltages are required: one for the gates and another for the drains, which is an improvement over the circuit in Fig. 5.5(a) which needs four different dc bias voltages. Measured results for the circuit in Fig. 5.5(b) reveal a conversion loss of 5–7 dB over an output signal band of 30–50 GHz using an RF input power level of +10 dBm. The fundamental rejection was above 13 dB and the third harmonic rejection was above 25 dB.

5.5 Mixers with Internal LO Frequency Multiplication

Since multipliers are commonly used to generate the harmonic of an LO signal which is then fed to a mixer circuit, much work has been devoted to incorporating the LO multiplication and mixing processes into a single circuit and thereby perform both operations at once. These specialized mixer circuits are often referred to as subharmonic mixers and usually the LO signal is internally multiplied by a factor of 2 or 4, but higher values are also possible.

Diode-based subharmonic mixers use an anti-parallel diode pair as its basic building block, as shown in Fig. 5.6. The LO and RF signals are fed to the mixer through a set of bandpass filters. It is common practice to design these two bandpass filters concurrently using diplexer design techniques [14]. A lowpass filter is used at the IF port and this one can be designed fairly independently from the other two filters since the IF signal is at a much lower frequency.

To see how the circuit in Fig. 5.6 behaves simultaneously as a frequency mixer and multiplier, we analyze the current flows in the diode pair. The currents i_1 and i_2 in Fig. 5.6 are given by the following expressions,

$$i_1 = I_o\left(e^{v_p/nV_T} - 1\right) \quad \text{and} \quad i_2 = I_o\left(e^{-v_p/nV_T} - 1\right) \tag{5.8}$$

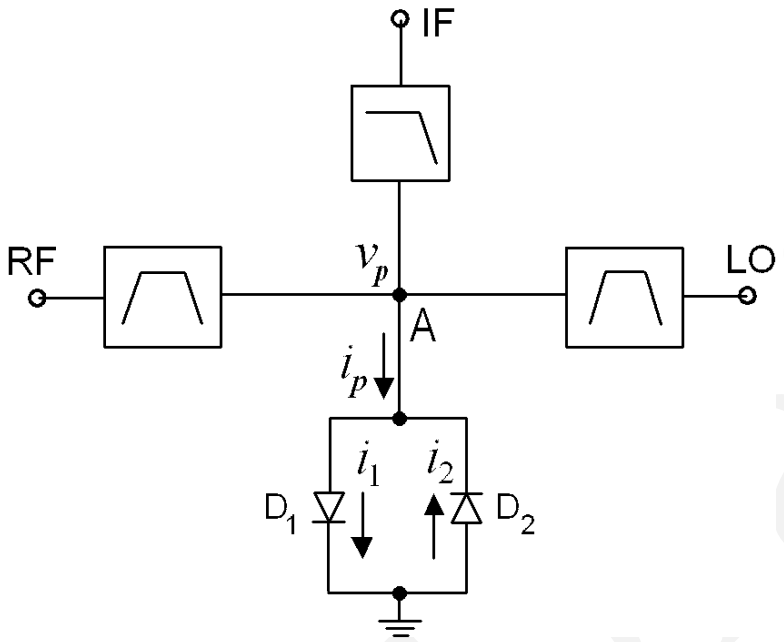

Figure 5.6: Subharmonic mixer using an anti-parallel diode pair

where v_p is the voltage drop across the diodes at node A, I_o is the diode saturation current, n is the diode ideality factor, and V_T is the device thermal voltage. The negative sign in the exponential term of i_2 is caused by the fact that the terminals of diode D_2 are reversed relative to D_1. This negative exponential term is the key to subharmonic mixing in this circuit structure. Peforming KCL at node A leads to $i_p = i_1 - i_2$ and after simplifying we obtain,

$$i_p = I_o \left(e^{v_p/nV_T} - e^{-v_p/nV_T} \right). \tag{5.9}$$

Using the Taylor series expansion, $e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \cdots + \frac{x^n}{n!}$, and keeping the terms up to the third power, Eqn. 5.9 becomes,

$$i_p = I_o \left[2 \left(\frac{v_p}{nV_T} \right) + \frac{1}{3} \left(\frac{v_p}{nV_T} \right)^3 \right] \tag{5.10}$$

The voltage v_p at node A in Fig. 5.6 is the superposition of the LO and RF input voltages, $v_p = v_{rf} + v_{lo}$. Note that in Eqn. 5.10 the squared term is absent, which is the term that

would lead to the mixing behavor in a fundamental mixer. Instead, there is a cubic term and if we examine the signals generated by it we observe that,

$$\frac{1}{3}\left(\frac{v_p}{nV_T}\right)^3 = \frac{1}{3n^3V_T^3}(v_{rf}^3 + 3v_{rf}^2 v_{lo} + 3v_{rf}v_{lo}^2 + v_{lo}^3). \tag{5.11}$$

If we let $v_{rf} = A_{rf}\cos(\omega_{rf}t)$ and $v_{lo} = A_{lo}\cos(\omega_{lo}t)$ then the $\frac{1}{n^3V_T^3}(v_{rf}v_{lo}^2)$ term in Eqn. 5.11 produces the following signals,

$$(1/n^3V_T^3)v_{rf}v_{lo}^2 = (1/4n^3V_T^3)A_{rf}A_{lo}^2\cos(\omega_{rf} \pm 2\omega_{lo})t + (1/2n^3V_T^3)A_{lo}A_{rf}\cos(\omega_{rf}t). \tag{5.12}$$

We see in this last expression that the mixer produces an upconverted and a downconverted frequency at $\omega_{rf} + 2\omega_{lo}$ and $\omega_{rf} - 2\omega_{lo}$, respectively, and in both cases the LO signal is multiplied by a factor of 2, as desired. Using the anti-parallel diode topology it is also possible to get even higher LO multiplication factors such as $\times 4$. If the Taylor series expansion used in Eqn. 5.10 were carried out to the 5^{th} power then one would observe output mixing frequencies of the type $\omega_{rf} \pm 4\omega_{lo}$. However, the conversion loss of the subharmonic mixer at the higher multiplication factors is significantly more than for the $\times 2$ case.

A number of different subharmonic mixers have been been demonstrated using FET and bipolar devices and they come in both passive and active versions. The passive FET subharmonic mixers usually rely on a ring mixer device topology in which the switches are replaced by $\times 2$ frequency doublers [15] [16]. Here we will focus on active subharmonic mixers based on the Gilbert-cell topology because they offer conversion *gain* and they have high spurious signal rejection. While the benefit of having conversion gain comes at the cost of DC power consumption, this is mitigated by not needing an amplifier stage after the mixer to compensate for conversion loss as is the case with passive mixers.

Fig. 5.7(a) shows the basic Gilbert-cell mixer structure [17]. It is a fundamental-mode mixer, meaning that its output mixing frequencies are $\omega_{if} = \omega_{rf} \pm \omega_{lo}$. Transistors M_1 and

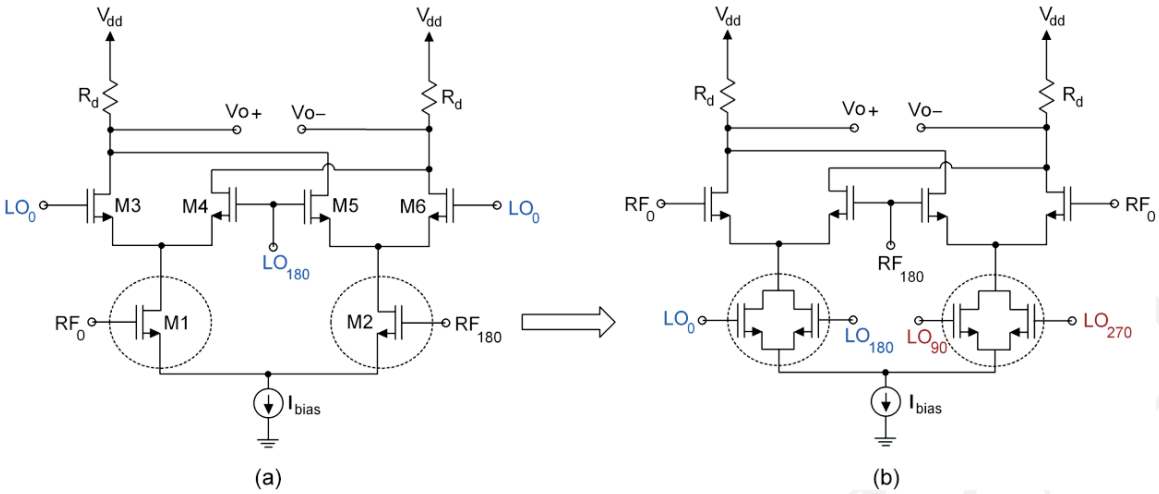

Figure 5.7: (a) Fundamental-mode Gilbert-Cell mixer (b) subharmonic variant

M_2 are a differential transconductance stage that convert the RF input voltages into currents. These currents are fed to a network of transistors that are driven by a differential LO signal. The LO transistors are driven to fully turn on and off, thereby acting as switches that chop the RF currents, which leads to the mixing behavior of the circuit. The two identical load resistors, R_d, convert the mixer output current back to voltage and their values can be chosen to provide conversion gain. Since all three ports of the mixer are differential, this accounts for its excellent spurious rejection and port-to-port isolation. The double-sideband noise figure of the mixer in Fig. 5.7(a) is usually above 10 or 12 dB, which is somewhat high. However, the noise performance can be significantly improved and brought below 6 dB by using very low-noise RF transconductance stages in the mixer [18] [19].

The fundamental-mode Gilbert-cell mixer in Fig. 5.7(a) can be converted into a $\times 2$ subharmonic mixer by replacing devices M_1 and M_2 with frequency doubler circuits as shown in Fig. 5.7(b). Note that the LO and RF input terminals in the subharmonic mixer have been flipped relative to the fundamental mixer. Without this change in the input ports, one would need to replace all the LO transistors in Fig. 5.7(a) with doublers, requiring four extra devices in the subharmonic version. Not only would this increase the DC consumption

of the subharmonic mixer, but more importantly it would require more LO signal power to drive the mixer. Instead, by flipping the input terminals, only two extra devices are needed.

The subharmonic mixer uses quadtrature LO signals and this stems from the fact that since the input signal is $v_{lo} = A_{lo}\cos(\omega_{lo}t + n\frac{\pi}{2})$ where $n = 0, 1, 2, 3$, and upon multiplying the frequency by 2 it leads to a new LO signal of the type $v_{2lo} = A_{2lo}\cos(2\omega_{lo}t + n\pi)$. The new LO signal at twice the frequency has only two phase angles, 0 and π, as desired. A passive on-chip polyphase network can be used to generate the quadrature LO signals without needing too much die area. In high performance applications where high spectral purity LO signals are needed and in which chip area and DC power consumption might be less of a concern, a quadrature voltage-controlled oscillator can be used instead.

For the same RF and LO input power levels and dc bias levels, the subharmonic Gilbert-cell mixer will generally have a lower conversion gain than the fundamental mixer. This is not unexpected, since the doubling operation in the LO path of the subharmonic mixer will subtract from its conversion gain. An expression to predict the conversion gain of the subharmonic mixer under discussion has been derived in [10],

$$CG = 20\log\left[\frac{R_d A_{lo} I_{bias}}{4(V_{GS(RF)} - V_t)(V_{GS(LO)} - V_t)^2}\right] \tag{5.13}$$

where V_t is the threshold voltage of the transistors, $V_{GS(RF)}$ is the gate-to-source dc voltage of the RF devices and similarly $V_{GS(LO)}$ is the gate-to-source dc voltage of the LO devices.

The measured conversion gain for these mixers is typically between 8 dB and 12 dB and they have a $P_{1dB,out}$ of about 0 dBm [20] [21] [22]. The port-to-port isolation in a subharmonic mixer is usually quoted for both the LO-RF and 2LO-RF cases, since both the fundamental and 2^{nd} harmonic LO signals can feed-through to the RF port. The LO-RF isolation can reach into the 65-70 dB range while the 2LO-RF isolation is typically about 10 dB lower than this. A similar behavior is observed for the LO feed-through measured at the

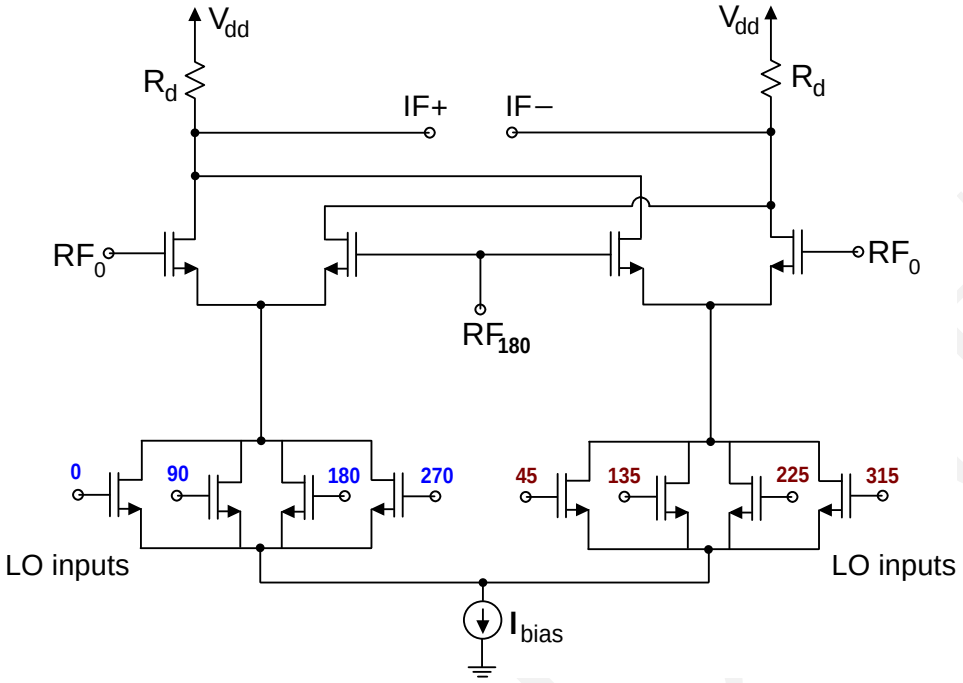

Figure 5.8: ×4 CMOS subharmonic mixer

IF port.

The circuit in Fig. 5.7(b) can be transformed into a ×4 subharmonic mixer by doing further work on the LO multiplication network. Shown in Fig. 5.8 is the first known active ×4 subharmonic mixer in CMOS [23]. To generate the $4\omega_{lo}$ frequency, eight transistors are used in the LO network and these devices are driven by octet phase signals. In other words, the LO input waveforms are now of the type $v_{lo} = A_{lo}\cos(\omega_{lo}t + n\frac{\pi}{4})$ where $n = 0, 1, 2 \ldots, 7$. At the 4^{th} harmonic we then have $v_{4lo} = A_{4lo}\cos(4\omega_{lo}t + n\pi)$ and the phases are once again 0 and π as required.

This ×4 mixer exhibits a measured conversion gain of 5.8 dB, which is the highest gain for a ×4 subharmonic mixer of any type reported in the literature to date. The mixer's LO-RF and 4LO-RF isolations are 71 dB and 59 dB respectively, and also, its LO-IF isolation is 68 dB and its 4LO-IF isolation is 59 dB. Since the LO is multiplied by a factor of 4, this means that the LO self-mixing performance of this mixer is expected to be very good.

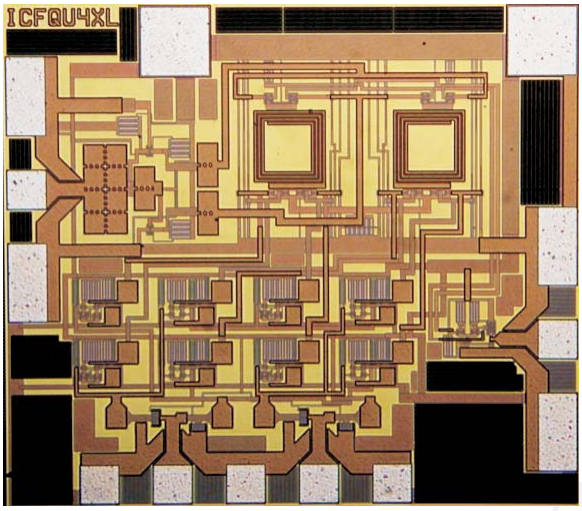

Figure 5.9: ×4 CMOS subharmonic mixer microphotograph. From [23] Copyright © IEEE 2008.

Indeed, measurements reveal that for a +10 dBm LO input signal (V_{rms} = 707 mV), the measured dc self-mixing voltage at the IF port is only 4.2 mV, which represents a "rejection" of 20log(707/4.2) = 45 dB. A microphotograph of the chip is shown in Fig. 5.9. For further details on this mixer, see [23].

5.6 Odd-order Frequency Multipliers

The recurring theme of this chapter has been that frequency multiplication occurs when a periodic signal enters a non-linear circuit which then generates harmonics of the fundamental. It is normally the case that the power in the harmonics decreases as the harmonic number, or index, increases. Consider a primitive multiplier in which a sinusoidal signal, $v_{in} = A_{in}\cos(\omega t)$, is incident on a single diode whose I-V curve of the type $i = I_o(e^{v_{in}/nV_T} - 1)$. The power series expansion of the diode output current is simply,

$$i = I_o\left[\frac{v_{in}}{nV_T} + \frac{1}{2!}\left(\frac{v_{in}}{nV_T}\right)^2 + \frac{1}{3!}\left(\frac{v_{in}}{nV_T}\right)^3 + \frac{1}{4!}\left(\frac{v_{in}}{nV_T}\right)^4 + \cdots\right]. \tag{5.14}$$

Frequency	Output Amplitude	dBc
ω	1	0
2ω	$\frac{1}{4}$	-12.0
3ω	$\frac{1}{24}$	-27.6
4ω	$\frac{1}{192}$	-45.7

Table 5.1: Harmonic frequency amplitudes

If we let $A_{in} \equiv nV_T$, for illustrative purposes, then we can determine the amplitudes of the output frequencies with the aid in Eqn. 5.14 and some trigonometric manipulations. The resulting amplitudes, normalized relative to the fundamental, are shown in Table 5.1. The table illustrates the general idea that using a single diode to generate frequencies above the second harmonic is usually not the preferred method[1]. For instance, using one diode to generate the 4ω signal would mean having to sustain an unacceptable loss of -45.7 dB relative to the fundamental. A straightforward, but effective, solution to reduce the conversion loss in $\times 4$ diode mulitipliers is to design a $\times 2$ multiplier and put two of those in series to get the 4ω signal. The overall conversion loss in this case would be: -12 dB - 12 dB = -24 dB instead of -45.7 dB.

To generate the odd-order harmonics such as the 3ω signal, one cannot use the same trick that was used for the 4ω frequency because the diode does not produce a 1.5ω signal that can be doubled. In fact, there are fewer odd-order multiplier designs reported in the research literature than even-order (2^n) multipliers precisely because they are not as convenient to design from lower-frequency harmonics.

A widely used tripler configuration for millimeter and submillimeter-wave applications is based on the anti-parallel diode pair that was discussed in the previous section (see Fig. 5.6). From Eqn. 5.10, which is the expression that describes the current-voltage relationship

[1]The exception to this observation is when specialized Step-Recovery Diodes are used for harmonic generation [24].

of the diode pair, we see that the circuit has a cubic term and no even-order terms. The 3ω signal will be 6 dB higher if it is generated by an anti-parallel diode pair as opposed to a single diode, which is easily verified by calculating the signal amplitudes using Eqn. 5.10 and Eqn. 5.14.

The anti-parallel diode pair is attractive due to its simplicity and very high-frequency capabilities [25] [26] [27]. At the lower end of the microwave spectrum, a larger number of tripler design concepts can be implemented with transistors. Many transistor-based triplers function on the principle of overdriving the device so that the output waveform is a clipped sinusoid that is rich in harmonics (see Fig. 5.10a). Power amplifier topologies have been used to achieve this aim, and it has been found that to improve the conversion efficiency of the tripler the devices should be biased for Class B or Class AB operation [28] [29]. Invariably, these tripler circuits need either a filter or special stub matching at the output to separate the desired triple frequency from the unwanted harmonics, both of which can result in fairly large chip areas.

A recent advance in tripler design involves a very different and innovative method that relies on the idea of making a deep cut into each wave peak of the fundamental signal in the time domain, leading to an output waveform with a strong third order harmonic [9]. Since this method relies on time-domain manipulation of the input signal waveform, it can be thought of as a "waveshaping" technique. Fig. 5.10 shows a pair of sketches depicting (a) the well known method of clipping a sinsouid to generate multiple harmonics and (b) the new waveshaping technique. Because the waveform in Fig. 5.10(b) more clearly resembles a triple frequency signal, this means that a less stringent, lower-Q, filter can be used at the output to isolate the third harmonic as compared to the clipping technique shown in Fig. 5.10(a).

A detailed schematic of the waveshaping tripler circuit is shown in Fig. 5.11. The key

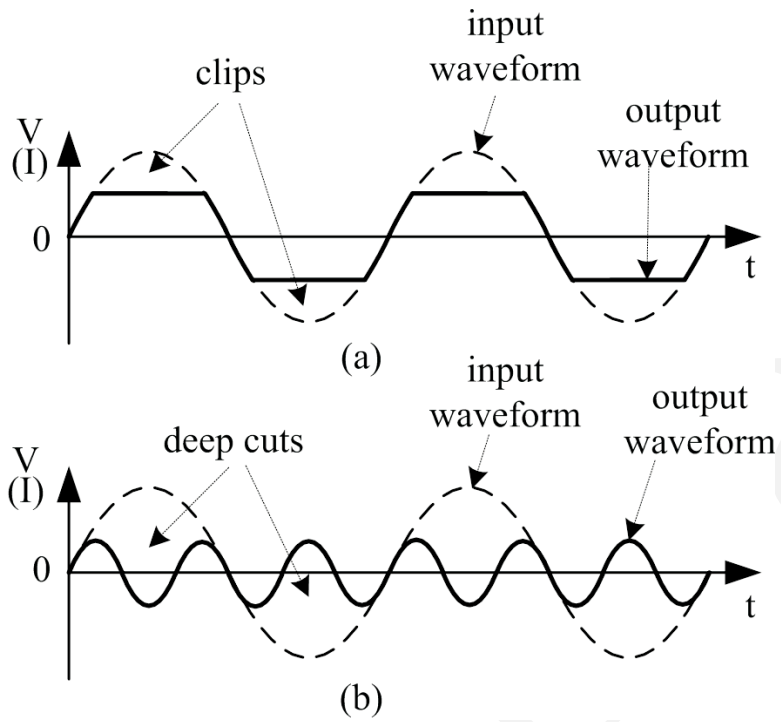

Figure 5.10: Creating a triple frequency by (a) clipping a sinusoid to generate multiple harmonics and (b) making deep-cuts in the fundamental signal. From [9] Copyright © IEEE 2007.

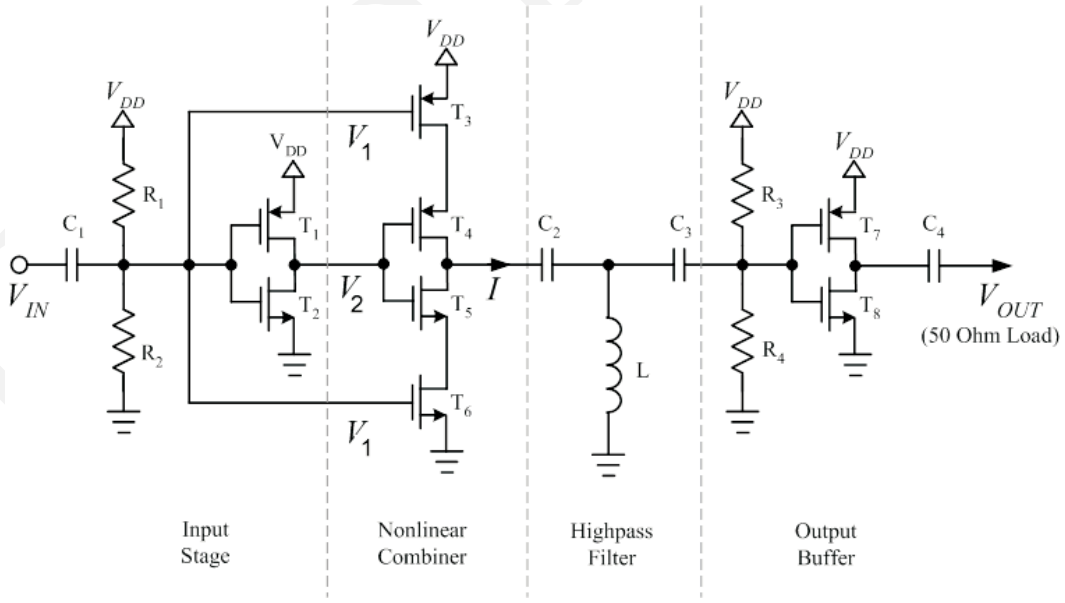

Figure 5.11: Waveshaping frequency tripler circuit implementation. From [9] Copyright © IEEE 2007.

concept behind this circuit is to take the input fundamental signal, $V_{IN} \equiv V_1$, and combine it with an inverted version of itself, V_2, in order to create the deep cuts in the fundamental waveform as depicted in Fig. 5.12. Transistors T_1/T_2 constitute an inverting amplifier to generate the signal V_2 and transistors T_3 through T_6 are a nonlinear combining structure that take V_1 and V_2 as inputs and yield an output current, I, taken at the drains of T_4/T_5 and which has a strong third harmonic. The signal V_2 cancells V_1 only at the postitive and negative peaks of V_1 in order to produce the deep cuts. However, in the middle region between t_2 and t_3 in Fig. 5.12(b), V_2 and V_1 are combined in an *additive* manner so that the signals reinforce each other in those time intervals. Note that this process is quite different from a simple linear combination of V_1 and V_2, which would produce a trivial output signal of the type $V_1 + V_2 = A_1 \cos(\omega t) + A_2 \cos(\omega t + \pi) = (A_1 - A_2) \cos(\omega t)$, which does not have any harmonics.

Transistors T_3/T_6 form an inverter (I) that is driven by V_1 and T_4/T_5 is a second inverter (II) nested within the first inverter whose input is V_2. Inverter 1 operates between two threshold voltages, TH_1 and TH_4, and since the amplitude of V_1 is kept between these two voltages as shown in Fig. 5.12(a), inverter 1 is on during the entire wave cycle of V_1. Inverter 2 has a different set of threshold voltages, TH_2 and TH_3, which fall between TH_1 and TH_4 as depicted in Fig. 5.12(b). For the time period $t = 0$ to t_1, inverter 2 is on and the output current I is in the upswing. From t_1 to t_2 the signal V_2 is outside the threshold voltages of inverter II, and therefore this inverter is off, leading to a decrease in the output current, I. This decrease in the output current occurs during a peak of V_2, which is also a (low) peak of the input signal. A similar process occurs for the time period t_3 to t_4 and this is how the deep cuts in the fundamental waveform are achieved.

Since the output current, I, from the nonlinear combining network has a strong third harmonic, this means that a relatively simple on-chip filter can be used to clean up the output waveform from the tripler. The circuit in Fig. 5.11 uses just a three-element highpass filter

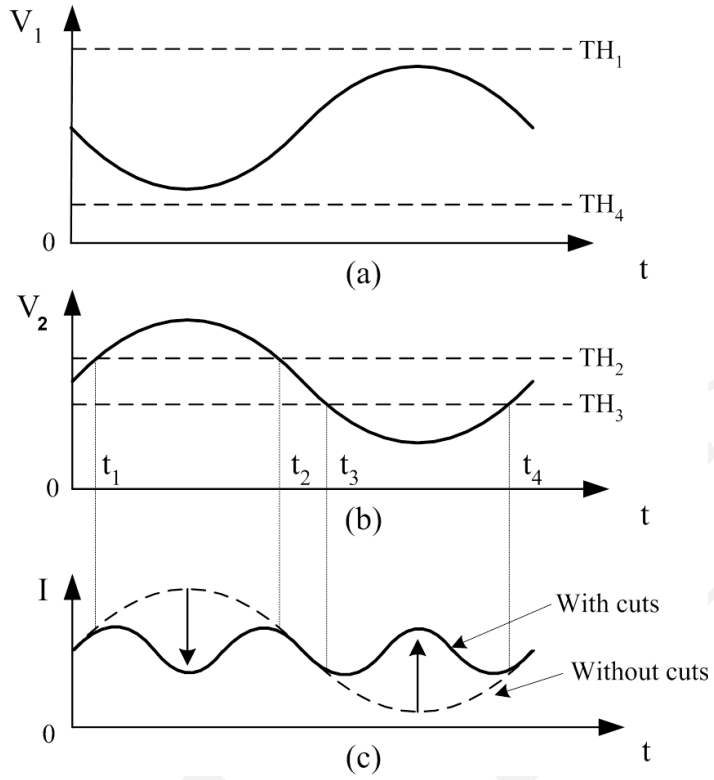

Figure 5.12: Waveshaping process: (a) the input fundamental waveform V_1 (b) the inverted waveform V_2 and (c) nonlinear combination of V_1 and V_2 to enhance the third harmonic. From [9] Copyright © IEEE 2007.

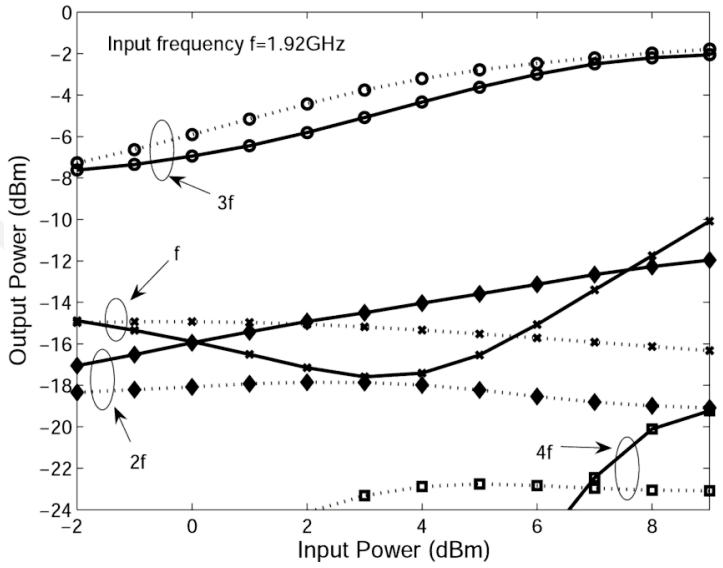

Figure 5.13: Measured power response for the tripler using the waveshaping technique. From [9] Copyright © IEEE 2007.

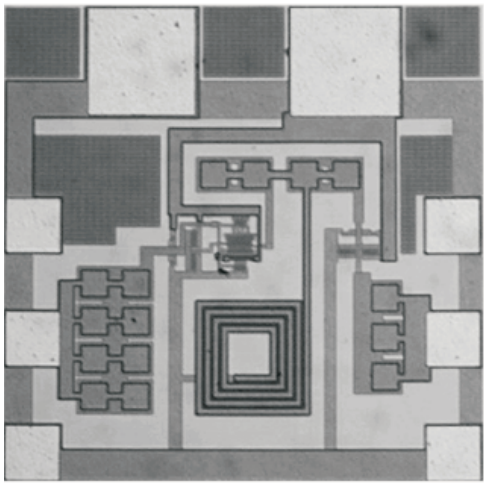

Figure 5.14: Tripler microphotograph. From [9] Copyright © IEEE 2007.

to reject the fundamental tone. Fig. 5.13 shows the measured harmonic power response for this multiplier [9]. The conversion loss for the triple frequency is 5.6 dB for an input power of -2 dBm at 1.92 GHz. The supperssion of the fundamental and second harmonic is around 10 dB or better and the fourth harmonic rejection is above 20 dB. The chip measures only 0.08 mm^2, excluding bonding pads, and consumes 27 mW of dc power in a 0.18-μm CMOS process. A microphotograph of the chip is shown in Fig. 5.14

Another tripler circuit that is also compact because it even avoids the use of any filtering structures altogether is described in [10], and its block diagram is shown in Fig. 5.15. The incident signal, ω_{in}, is fed to both inputs of a $\times 2$ subharmonic mixer to generate the output frequencies $3\omega_{in}$ and ω_{in}. In addition, the circuit includes a feedforward mechanism to cancel the ω_{in} signal at the output, leaving only the $3\omega_{in}$ signal. A variable phase shifter is used in the feedforward path in order to produce the precise 180° phase shift needed at the summing junction for maximum fundamental signal cancellation. An amplifier is also included in the feedforward path because the signal amplitudes have to be matched as well. The subharmonic mixer used for this tripler was identical to the one shown in Fig. 5.7(b). Since the constituent subharmonic mixer has a positive conversion gain then the tripler

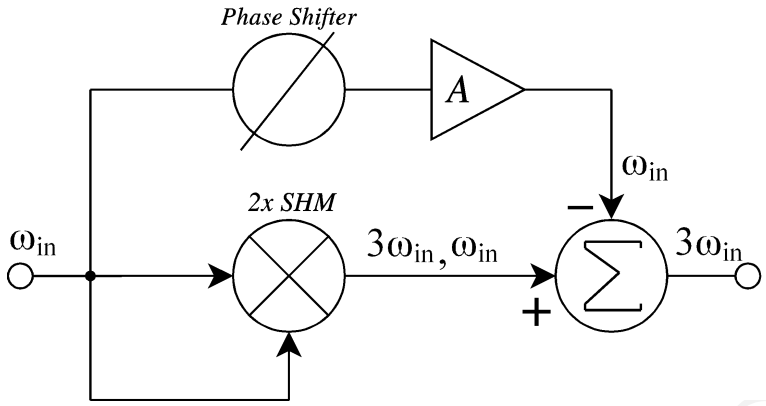

Figure 5.15: Frequency tripler using a CMOS subharmonic mixer and including feedforward fundamental cancellation. From [10] Copyright © 2009 IEEE.

circuit is also expected to have conversion gain, which it does. The measured gain of the tripler is 3.0 dB using a -10 dBm input signal at 1 GHz.

The subcircuit used for the feedforward cancellation is shown in Fig. 5.16. At its core is a subtractor circuit which is a just a differential amplifier. The output of the subtractor is taken single-ended, meaning that the output voltage is $v_o = \frac{g_m}{2}(v_{SHM} - v_{FF})$, where v_{SHM} is the signal from the subharmonic mixer after its converted to single-ended form by the balun circuit, and v_{FF} is the fundamental signal produced by the feedforward circuit. The experimental results in Figs. 5.17–5.18 show that using this signal cancellation method leads to a high fundamental signal rejection of 30 dB at the output relative to the desired third harmonic when the RF input power level is around -10 dBm.

The internal doubling operation in the subharmonic mixer used in this triper produces even harmonics of the ω_{in} signal. However, these even harmonics are eventually multiplied with ω_{in} itself leading to only odd harmonics. Mathematically we can write this as,

$$v_{mix} = \sum_{n=1}^{\infty} a_n \cos(2n\omega_{in}t)\cos(\omega_{in}t) \tag{5.15}$$

$$= \sum_{n=1}^{\infty} b_n \cos((2n \pm 1)\omega_{in}t). \tag{5.16}$$

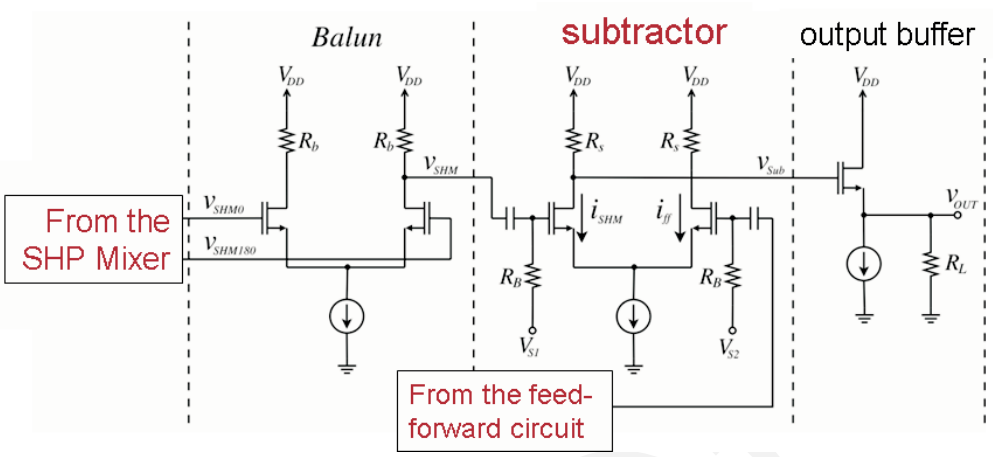

Figure 5.16: Fundamental cancellation circuit

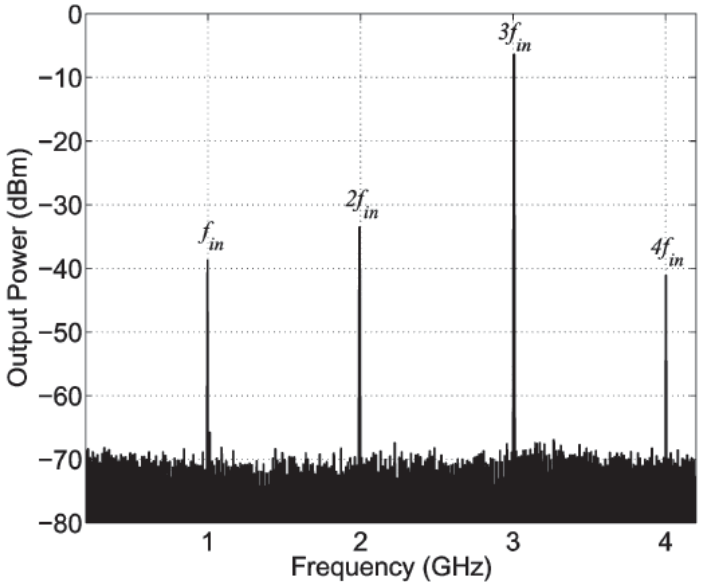

Figure 5.17: Measured spectral response of the tripler with feedforward cancellation. From [10] Copyright © 2009 IEEE.

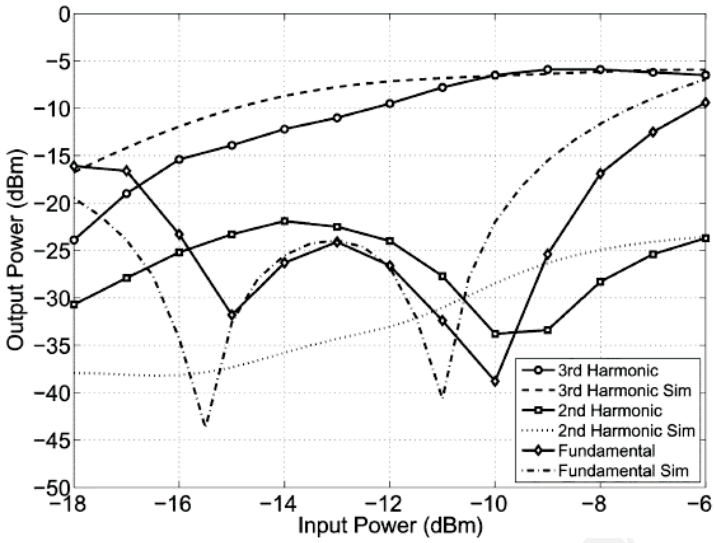

Figure 5.18: Measured power response of the tripler with feedforward cancellation. From [10] Copyright © 2009 IEEE.

The measured spectra of this tripler shows that the even harmonics are well rejected without the need for any filters on or off-chip, thus leading to a very compact IC measuring only 0.8 mm^2. A microphotograph of the chip is shown in Fig. 5.19.

5.7 Conclusion

Frequency multiplication plays a key role in signal generation in the microwave and millimeter-wave region of the spectrum. While single-transistor multipliers are suitable for implementing frequency doublers, more advanced techniques are required for frequency tripler in order to maintain the conversion loss at acceptably small levels. Recent advances in tripler design have used the concept of manipulating the shape of the incident waveform so that the output signal has a strong third harmonic. Another method has relied on a $\times 2$ subharmonic mixer to generate the triple frequency. A key feature of these new circuit concepts is that off-chip filters are eliminated thus leading to very compact IC designs.

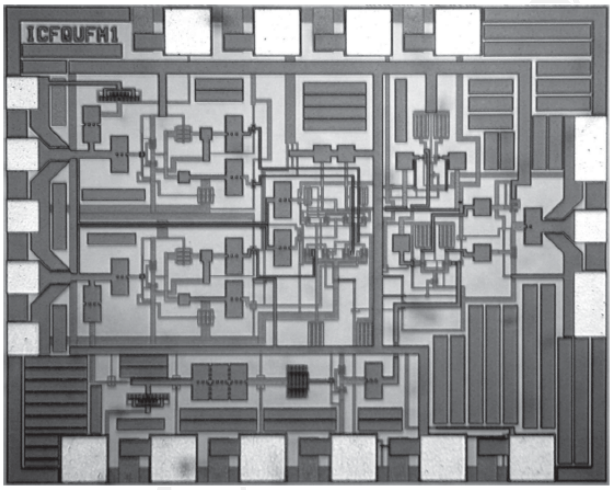

Figure 5.19: Microphotograph of the fabricated tripler. From [10] Copyright © 2009 IEEE.

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