A CMOS Broadband Low-Noise Mixer With Noise Cancellation

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***Abstract*—This paper presents a broadband low-noise mixer in CMOS 0.13-μm technology that operates between 1–5.5 GHz. The mixer has a Gilbert cell configuration that employs broadband low-noise transconductors designed using the noise-cancelling technique used in low-noise amplifer designs. This method allows broadband input matching and without the use of inductors that are frequently required in low-noise mixer designs. The current-bleeding technique is also used so that a high conversion gain can be achieved. Measured results show excellent noise and gain performance across the frequency span with an average double-sideband noise figure of 3.9 dB and a conversion gain of 17.5 dB. It has a third-order intermodulation intercept point of +0.84 dBm at 5 GHz and it is also very compact with the size of the mixer core only being 0.315 mm^2.**

***Index Terms*—Broadband, CMOS mixer, current bleeding, low noise, low-noise amplifier (LNA), multistandard, noise cancellation, RF integrated circuit (RFIC).**

I. Introduction

ACTIVE MIXERS based on the Gilbert cell configuration often exhibit a large amount of noise. This leads to strict requirements for the noise figure (NF) of the low-noise amplifier (LNA) preceding the mixer such that a particular signal-to-noise ratio can be achieved. This usually requires at least one very low-noise LNA that has enough gain and noise performance to mitigate the noise added by the mixer. Power consumption is also a problem as the LNA NF decreases when larger transistors are used. However, these requirements can be much relaxed or the LNA can be removed if the mixer NF is low enough. The Gilbert cell mixer has been widely used in integrated circuit (IC) design even though it exhibits moderate noise. However, its NF can be drastically reduced by combining the LNA and mixer into a single component. Narrowband low-noise mixers have been proposed in other works [1]–[4], where the transconductors were replaced by inductive-degenerated LNAs.

Currently, electronic devices are moving toward more functionalities in very compact sizes. More multiband multistandard devices are becoming available, such as multiregion cellphones with built-in Wi-Fi and a global positioning system (GPS). If narrowband mixers are used, they need to be designed individually to accommodate each frequency band. The complete multiband multistandard receiving system might have many branches, each for one frequency band. Not only does this architecture increase the overall system size and costs, but it also complicates the design process, especially with low-noise mixers, due to their narrowband nature and the number of inductors used. However, with a broadband low-noise mixer, the design of such a system can be much simplified. Due to the broadband and low-noise nature, the mixer can also find applications in software-defined radios (SDRs), as well as multiband ultra-wideband (UWB) systems.

To convert a Gilbert cell into a broadband low-noise mixer, the transconductors must be broadband in terms of NF, gain, and input match. Many broadband and UWB LNAs have been proposed [5]–[7]. In [5], an active feedback approach was used to achieve broadband matching and gain. The circuits in [6] and [7] use filters to achieve broadband input matching and low noise performance.

Another broadband LNA design method is the noise-cancelling technique [8]. It is appealing because no inductors are required, while a sub 3-dB NF is achievable. The circuit is, therefore, very compact and there is also broadband input matching. The technique can be used to cover a large bandwidth, as demonstrated in [9].

In this paper, a broadband low-noise mixer is presented using the LNA noise-cancelling concept to implement the transconductor stage of the Gilbert cell mixer. The LNA and mixer are, therefore, merged seamlessly into a single component. This current-reuse topology is very attractive because the mixer current is completely reused by the LNA. The large bandwidth and low NF of the mixer is very suitable in a multiband system. The mixer is designed to operate from between 1 to 5.5 GHz with a constant IF of 250 MHz and it compares very well in many performance metrics relative to other broadband mixers.

II. Circuit Description

The proposed broadband low-noise mixer block diagram is shown in Fig. 1. The mixer follows the Gilbert cell topology with some modifications. The mixer is comprised of three building blocks: noise-cancelling transconductors, a current-bleeding circuit, and switching pairs. A detailed design analysis of the noise-cancelling block is provided first, followed by a description of each block.

A. Noise-Cancelling Transconductors

Shown in Fig. 2 is the noise-cancelling transconductor stage of our mixer, which is based on the noise-cancelling LNA topologies used in [9] and [10]. Transistors M_1–M_3 form the transconductor, which turns the RF input voltage into RF currents. The common-gate (CG) transistor at the first stage is the input matching network since the impedance looking into the source is about $1/g_m$. The input impedance of M_3, which

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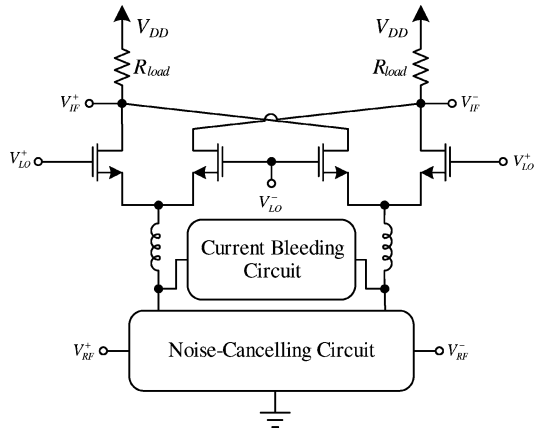

Fig. 1. Block diagram of the proposed mixing circuit.

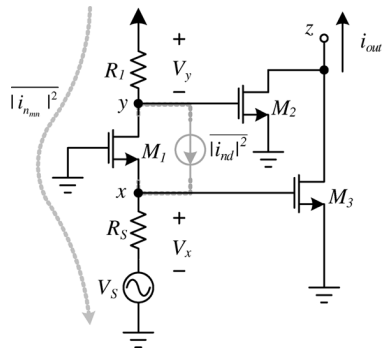

Fig. 2. Noise-cancelling transconductor.

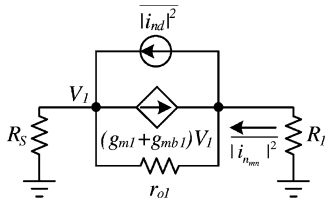

Fig. 3. CG small-signal model used to calculated total noise current flowing through the matching network.

has a common-source (CS) configuration, is large due to its $C_{\rm gs}$. Therefore, the input impedance of the circuit is dominated by M_1 at low frequencies. The noise generated from the CG matching network is high. Thus, a noise-cancelling circuit is placed after the matching circuit to cancel the noise and provide a high gain. The noise-cancelling circuit is comprised of two amplifiers (M_2 and M_3) in the CS configuration.

For the CG transistor, its noise sources can all be referred to the output and combined with the drain noise. The noise current $\overline{|i_{n_{mn}}|^2}$ in Fig. 2 is the total noise current flowing through the matching transistor from drain to source. Two nodes are defined here: node x and node y. The input matching circuit is a CG amplifier, therefore the signal voltage at node x and node y are in-phase. However, since the noise current of the amplifier flows through the transistor, the noise voltage at node x and node y are 180° out-of-phase. If a voltage adder is placed after the input matching stage, the signals at nodes x and y will be added, while the noise voltages will be subtracted. It should be noted that only the noise voltages caused by the transistor M_1 are cancelled. The noise coming from R_1 is not cancelled because its noise at node x and y are in-phase. It will be shown later how to minimize its noise contribution. Furthermore, the noise coming from the voltage adder is not cancelled. Thus, the adder must provide a high gain to reduce its noise contribution to the overall NF.

It can be seen that the noise current from M_1 at the output of the adder is

$$\begin{aligned}\overline{|i_{n_{mn}\rm out}|^2} &= \overline{|g_{m3}V_x - g_{m2}V_y|^2} \\ &= \overline{|i_{n_{mn}}|^2}(g_{m3}R_S - g_{m2}R_1)^2. \end{aligned} \tag{1}$$

Therefore, the noise from M_1 can be cancelled if $g_{m2} = (R_S/R_1)g_{m3}$, and when this condition is met, the noise from the noisiest component of the entire transconductor is eliminated. M_1's flicker noise, substrate noise, and thermal noise from the gate can all be cancelled as they can be referred to the output of the transistor.

For the adder, since the input matching constraint has been removed, the sizes of M_2 and M_3 can be chosen freely as long as the noise cancellation criteria holds. First, a large g_m is desired since it is directly proportional to the mixer gain. Thus, a large device size is preferable. In addition, a large g_m reduces the NF of the LNA. Second, the device size cannot be too big as the large $C_{\rm gs}$ of M_3 will affect the input match, rendering the input matching circuit useless. Furthermore, a large $C_{\rm gd}$ will affect the noise-cancelling ability of the adder. An undesired Miller effect will also affect the input matching network.

To quantify the above view, the NF of the transconductor is derived following a procedure similar to that of [10] with the difference that here we focus on noise *currents* instead of noise voltages. The body effect is also considered, as it affects noise performance and input matching. To simplify the analysis, $C_{\rm gd}$, and $C_{\rm gs}$ are not included. Furthermore, only the channel thermal noise of the transistors was considered, as the point of this analysis is to provide a design guideline for this particular circuit. The input impedance of the transconductor is roughly equal to the input impedance of the CG amplifier. The input impedance and effective transconductance of the transconductor are given by

$$Z_{\rm in} \approx \frac{r_{o1} + R_1}{1 + (g_{m1} + g_{mb1})r_{o1}} \tag{2}$$

$$g_{m_{\rm eff}} = g_{m3} + g_{m2}\left[\frac{1 + (g_{m1} + g_{mb1})r_{o1}}{1 + \frac{r_{o1}}{R_1}}\right] \tag{3}$$

where g_{mb1} is due to the body effect from transistor M_1. To calculate the noise current $\overline{|i_{n_{mn}}|^2}$, the small-signal model in Fig. 3 is used and can be expressed by

$$i_{n_{mn}} = \frac{i_{nd}}{1 + \frac{R_1 + R_S}{r_{o1}} + (g_{m1} + g_{mb1})R_S}. \tag{4}$$

The total noise current at the output due to the transconductor is, therefore,

$$\begin{aligned}\overline{|i_{nt_{\rm added}}|^2} = {g_{m2}}^2 4kTR_1 + \frac{4kT\gamma}{\alpha}(g_{m2} + g_{m3}) \\ + \overline{|i_{n_{mn}}|^2}(g_{m3}R_S - g_{m2}R_1)^2 \end{aligned} \tag{5}$$

where the first term is the noise contribution from R_1 and the second term is from M_2 and M_3. The noise current at the output due to the noise at the input from R_S is

$$\overline{|i_{n\mathrm{out_{in}}}|^2} = \frac{4kT}{R_S}(Z_{\mathrm{in}} \,\|\, R_S)^2 g_{m_{\mathrm{eff}}}. \tag{6}$$

The NF of the transconductor is

$$\begin{aligned} F &= 1 + \frac{\mathrm{Noise_{added}}}{G \cdot \mathrm{Noise_{in}}} \\ &= 1 + \frac{\overline{|i_{nt_{\mathrm{added}}}|^2}}{\overline{|i_{n\mathrm{out_{in}}}|^2}} \\ &= 1 + \frac{{g_{m2}}^2 R_1 + \frac{\gamma}{\alpha}(g_{m2}+g_{m3})}{\frac{1}{R_S}(Z_{\mathrm{in}} \,\|\, R_S)^2 {g_{m_{\mathrm{eff}}}}^2} \\ &\quad + \frac{\gamma}{\alpha} \frac{\frac{g_{m1}}{\left(1+\frac{R_1+R_S}{r_{o1}}+(g_{m1}+g_{mb1})R_S\right)^2}(g_{m3}R_S - g_{m2}R_1)^2}{\frac{1}{R_S}(Z_{\mathrm{in}} \,\|\, R_S)^2 {g_{m_{\mathrm{eff}}}}^2}. \end{aligned} \tag{7}$$

To simplify (7), it is assumed there is perfect cancellation, which means $g_{m2} = (g_{m3}R_S)/R_1$, and there is a perfect input match such that $Z_{\mathrm{in}} \approx 1/(g_{m1} + g_{mb1}) = R_S$. The simplified expression is

$$F = 1 + \frac{R_S}{R_1} + \frac{\gamma}{\alpha}\left(\frac{R_S}{R_1} + 1\right)\frac{1}{g_{m3}R_S}. \tag{8}$$

The above equation provides a design guideline for this circuit. Since R_S is fixed, only the values of R_1 and g_{m3} can be changed. R_1 should be made as big as possible to reduce its noise contribution. Care must be taken when sizing R_1 because (2) shows that a large R_1 affects input matching at low frequencies. The body effect is, therefore, desired for M_1 because a larger R_1 can be used while maintaining a good input match. The body effect also increases the overall gain and makes the noise-cancelling less sensitive to device mismatch and process variation, which is evident from (7). A large g_{m3}, which is directly related to g_{m2}, is preferred, as it not only provides a high gain, but also reduces the noise coming from M_2 and M_3. Again, they cannot be too large as C_{gs} from M_3 could ruin the input matching circuit. It should be noted that the above equation is only a first-order approximation as it ignores some high-frequency and noise parameters.

The layout for the transistors M_2 and M_3 is very important. Due to their large sizes, undesired noise coupling, as well as gate resistance noise and substrate noise, can be amplified and drastically increase the NF. The thermal noise from the polysilicon gates can be reduced by using multiple fingers and dual-connected gates. For a fixed total device width, more fingers translates to shorter per-finger width. By reducing individual finger width, the thermal resistance noise can be significantly reduced. However, there is an optimum point beyond which shrinking the per finger width will increase the transistor noise. This is caused by the gate–bulk capacitance (C_{gb}). By having more fingers, the number of contact pads, whose size is large relative to the gate length, increases [11]. If the gates are dual connected, the number of pads required is $2 \cdot N$, where N is the number of fingers. In this design, the optimum finger width in this technology was used. All of the gates are dual connected and triple wells are used for M_2 and M_3 to reduce substrate coupled noise. The body of M_1 is connected to ground to increase the body effect of the CG amplifier. In this CMOS technology, transistors M_2 and M_3 are biased with a 0.6-V gate voltage to achieve minimum NF for each transistor.

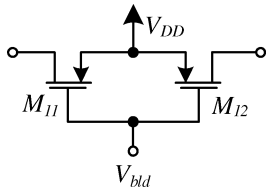

Fig. 4. PMOS bleeding circuit.

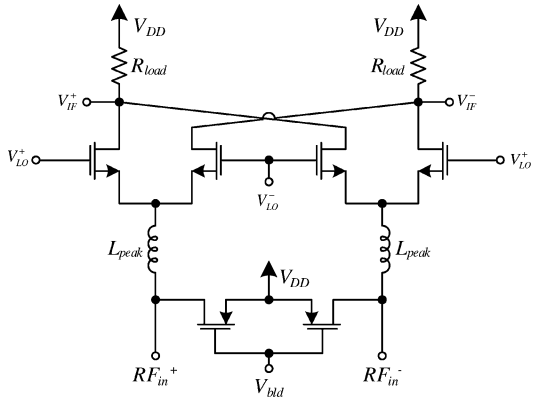

Fig. 5. Switching pairs with bleeding circuit and peaking inductors.

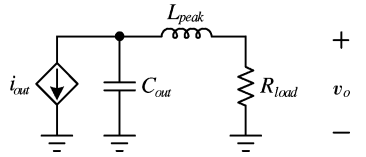

Fig. 6. Two-pole series peaking network.

B. Switching Pairs and Current-Bleeding

As explained in Section II-A, large M_2 and M_3 are desired in order to reduce their own noise contribution in the overall circuit. The amount of current draw subsequently increases and significantly reduces the load resistor size. A large overdrive voltage is also required for the switches to handle this current, making the switches less ideal. In order to have gain in this mixer, the current-bleeding circuit [12] is used to alleviate these problems. Fig. 4 is a typical bleeding circuit with two PMOS transistors providing dc current into the two transconductors. The PMOS pair provides a high output impedance that is in parallel with the small input impedance of the switching pair. Therefore, the weak RF signal is forced to go into the switching pairs.

The gain of the mixer is maximized with fast switching similar to a square wave. The turn-on voltage for the switching pairs is proportional to their overdrive voltage, and it needs to be low to ensure fast switching. With the bleeding circuit supplying most of the transconductors' current, the overdrive voltage can be reduced for better switching. By having a lower overdrive

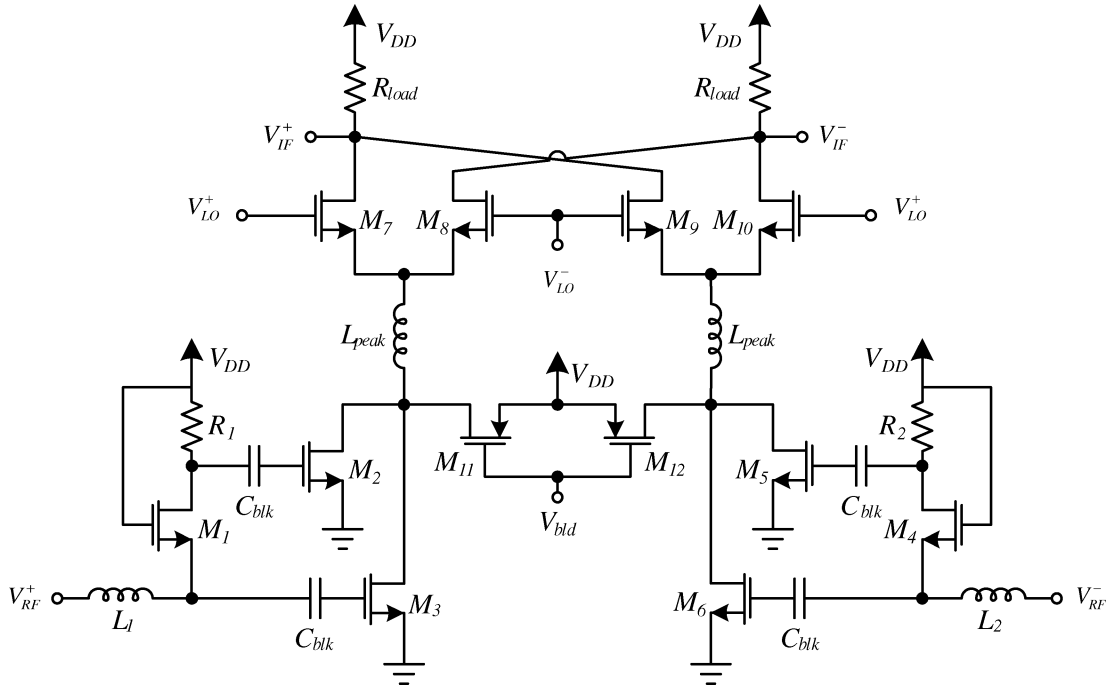

Fig. 7. Complete circuit schematic of the proposed mixing circuit.

voltage, the size of the load resistors can be increased to achieve an even higher gain.

C. Inductive Peaking

The mixer bandwidth can be significantly affected by the large output capacitance from M_2 and M_3, as well as from the bleeding circuit and switching pairs.

Inductive peaking can be used for bandwidth extension. Series peaking is used in this design and the peaking inductors $L_{\rm peak}$ are placed between the switching pairs and the current-bleeding circuit, as shown in Fig. 5.

To understand the purpose of these inductors, a simplified circuit is shown in Fig. 6 when only one of the switches is on. Preceding the mixer core is the transconductor, which can be approximated by a voltage-controlled current source; $C_{\rm out}$ is the collective output capacitance from the transconductor and the bleeding circuit; $R_{\rm load}$ is the mixer load resistor, assuming there is no loss through the switch, and the tail capacitance of the off switch is negligible compared to the load resistor.

The basic theory of inductive peaking can be explained with Fig. 6 and a step response. Imagine the circuit without the inductor, the rise time at the output is about $2.2RC$ if the rise time is defined to be the elapsed time between 10%–90% of the final output voltage value. To decrease the charge time, i.e., increase the bandwidth, the inductor is used. At $t = 0$, there is a sudden step change in the current source. The high impedance of the inductor decouples the resistor from the capacitor, which means all the current goes into charging the capacitor. Therefore, the rise time decreases, and hence, the bandwidth enhancement. This is also why the peaking inductors are placed in between the bleeding circuit and switching pairs, but not in between the transconductors and bleeding circuit.

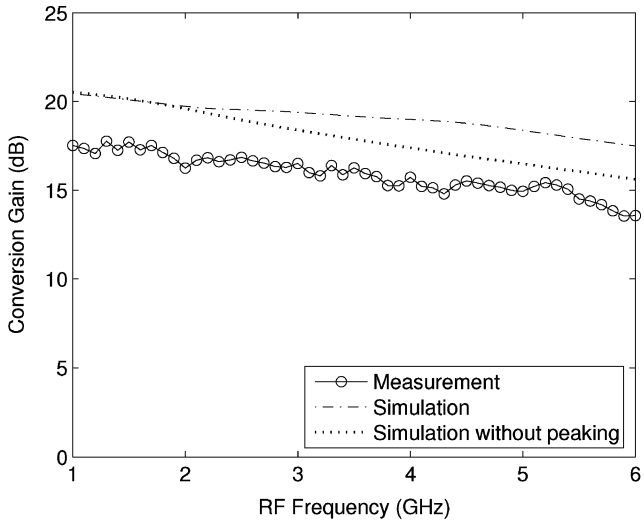

Fig. 8. Measured and simulated conversion gain of the mixer.

D. Complete Circuit

Fig. 7 shows the complete circuit of the noise-cancelling mixer. Inductors L_1 and L_2 are used in front of the transconductors to improve input matching. Shunt-and-series inductive peaking could have been used in the transconductors to further extend the bandwidth. However, the large number of inductors used increases the chip size. Furthermore, the number of inductors would be comparable to the UWB LNAs mentioned at the beginning of this section, making this noise-cancelling approach less attractive.

III. Simulation and Measurement Results

The mixer was designed using IBM's CMOS 0.13-μm technology. The layout was completed in Cadence and extracted by

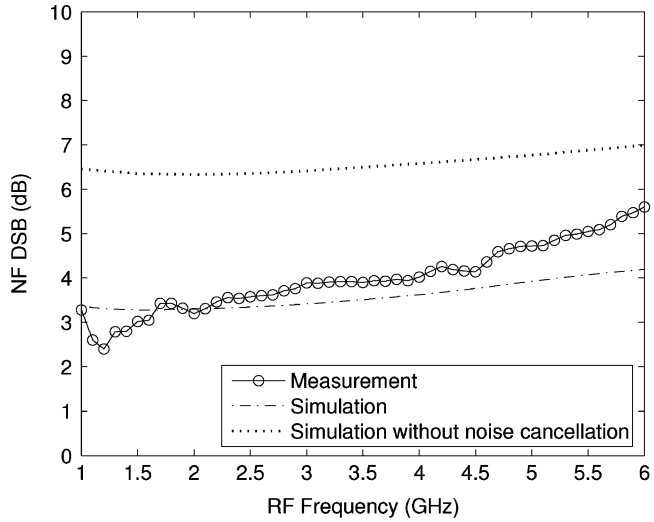

Fig. 9. DSB NF measurement and simulation results.

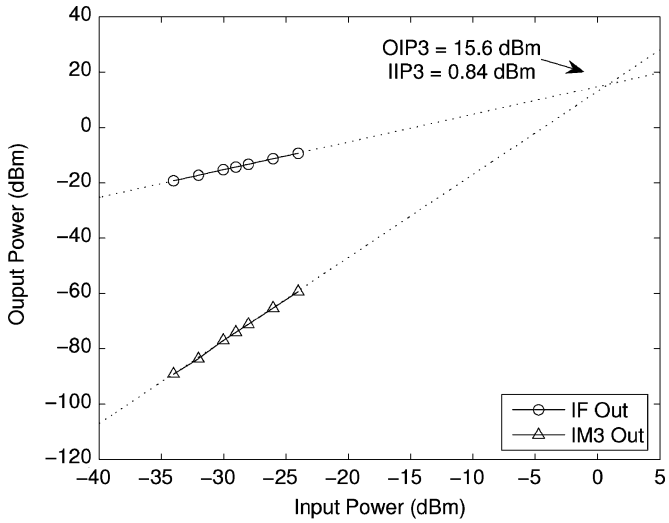

Fig. 10. Measured output powers of the IF and the IM3 product with the input at 5 GHz.

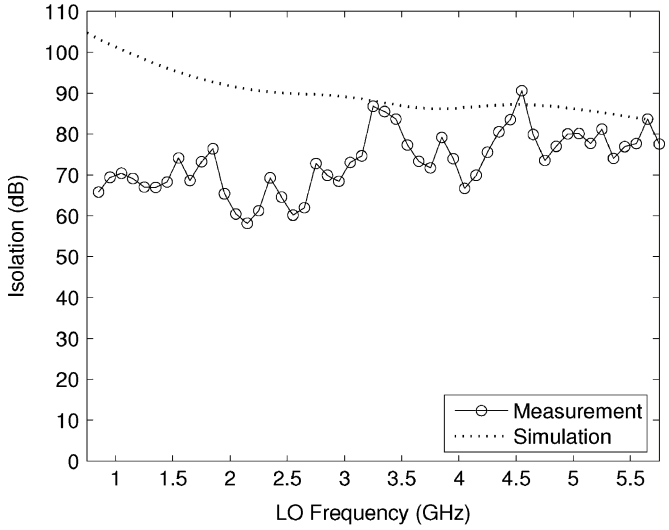

Fig. 11. LO-to-RF isolation from 0.75 to 5.75 GHz.

ASSURA using the *RC* option, which extracts both parasitic capacitance and resistance. Post-layout simulation was run using

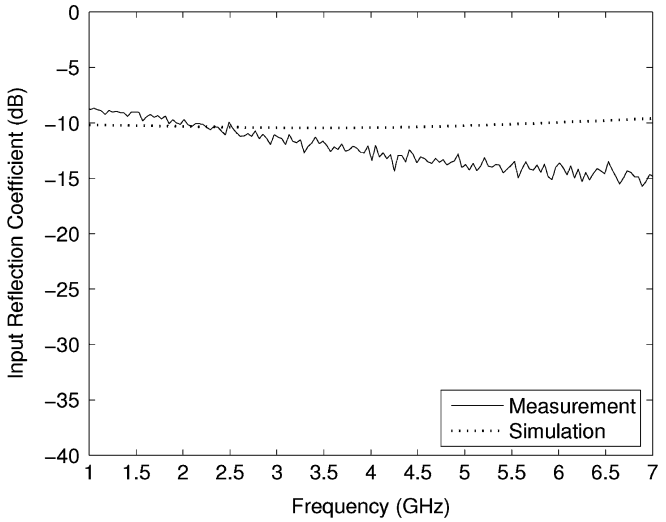

Fig. 12. Input reflection coefficient of the mixer.

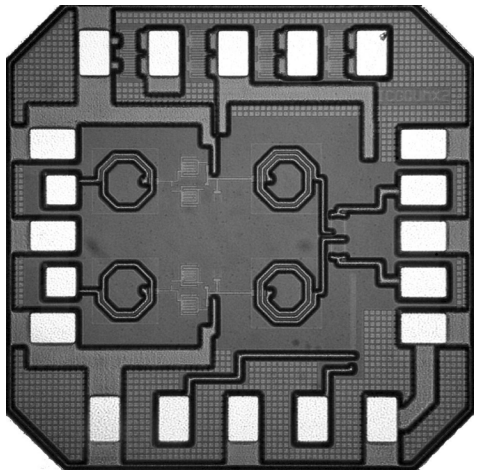

Fig. 13. Microphotograph of the chip.

Advanced Design System (ADS) through the Cadence-ADS Dynamic Link. The mixer is designed to operate between 1–5.5 GHz with a local oscillator (LO) power of 0 dBm. For all simulation and measurement results, the IF is always kept at a constant 250 MHz, while the RF and LO frequencies are being changed together with the LO being 250 MHz lower than the RF.

All three ports of the mixer are fully differential. On-wafer measurements were done using ground–signal–ground–signal–ground (GSGSG) coplanar waveguide probes. Since fully differential signals are required for the RF and LO, external 180° hybrids were used to convert the single-ended signals from the signal generators into fully differential signals. An off-chip buffer was used to combine the differential IF signal into a single-ended output.

The conversion gain of the mixer is measured across the input frequency ranging from 1 to 6 GHz. The input RF power was kept at −40 dBm. Fig. 8 shows the simulated and measured results. This plot also includes the simulated result without the peaking inductors. The importance of the peaking inductors can be clearly seen in this plot, where there is a much sharper gain rolloff compared to the simulated result with peaking.

TABLE I
COMPARISON OF BROADBAND DOWN-CONVERTERS WITH THIS WORK

Parameter	This Work Low Noise Mixer	[14] Blixer	[15] LNA + Mixer + TIA	[16] Folded LNA + Mixer
CMOS Technology	0.13 μm	65 nm	65 nm	90 nm
RF Frequency Span (GHz) 3 dB Bandwidth	$1-5.5$	$0.5-7$ 1 dB Bandwidth	$2-8$	$0.1-3.85$
Conversion Gain (dB)	17.5 (Power)	18 (Voltage)	23 (Voltage)	12.1 (Power)
NF (DSB) (dB)	3.9 (Average)	4.5–5.5	4.5	$8.4-11.5$ (SSB)
P_{1dB} (dBm)	-10.5	N/A	N/A	-12.83
IIP3 (dBm)	$+0.84$	-3	-7	N/A
LO – to – RF Isolation (dB)	>55	N/A	N/A	N/A
S_{11} (dB)	<-8.8	<-10	-8	<-10
Core Size (mm^2)	0.315	<0.01	0.09	0.88 with pads
Voltage Supply (V)	1.5	1.2	1.2	1.2
Power Consumption (mW)	34.5	16	39	9.8

The measured gain varies from 17.5 dB at 1 GHz to 13.6 dB at 6 GHz. The circuit operates between 1–5.5 GHz, which has a 3-dB bandwidth of 4.5 GHz. There is a roughly 3-dB difference in gain between simulation and measurement. The discrepancy is caused by the off-chip buffer that has some loading effect on the mixer output. Since no models were available for the buffer, it was not possible to include the effect of the buffer in the simulation. Nevertheless, it can be seen that both the simulated and measured gain responses share a similar shape even at very low frequencies.

When characterizing the noise performance of a mixer, either the double- or single-sideband NF can be used [13]. Fig. 9 shows the measured and simulated double-sideband NF ($\mathrm{NF_{DSB}}$) of the mixer versus frequency. The circuit has a low and relatively flat NF across a large 4.5-GHz bandwidth. The measured $\mathrm{NF_{DSB}}$ is below 3.5 and 4 dB for frequencies below 2.2 and 4 GHz, respectively. The absolute minimum $\mathrm{NF_{DSB}}$ is 2.4 dB at 1.2 GHz and the maximum $\mathrm{NF_{DSB}}$ is 5.1 dB at 5.5 GHz, with an average of 3.9 dB across the entire frequency range. There is a strong agreement between the measured and simulated results. The slope of the measured NF is higher than that of the simulated NF. Due to the noise cancellation nature of the mixer, undesired parasitics affect the noise cancellation ability of the mixer. Therefore, it is more pronounced at high frequencies; hence, the increase in slope. Fig. 9 also shows the simulated result without noise cancellation by disabling M_3, M_6, and the bleeding circuit. It shows that the noise-cancelling circuit reduces the NF by roughly 3 dB across the entire band.

The $P_{1\mathrm{dB}}$ and third-order intermodulation intercept point (IIP3) of the mixers were measured. To measure the IIP3, a two-tone signal separated by 1 MHz was used. Shown in Fig. 10 is the measured IF and third-order intermodulation (IM3) output powers with the input RF frequency at 5 GHz. The input referred $P_{1\mathrm{dB}}$ was -10.5 dBm and the extrapolated IIP3 was $+0.84$ dBm. The high IIP3 is due to the fact that the noise-cancelling mechanism also leads to a certain degree of distortion cancellation [10].

The LO-to-RF port-to-port isolation was measured. Since the LO is 250 MHz lower than the RF, the isolation was measured from 750 MHz to 5.75 GHz. Fig. 11 shows the measured and simulated LO-to-RF isolation, where it shows there is more than 55-dB isolation across the entire frequency range, and more than 60-dB isolation at most frequencies. The lower isolation at the low-frequency end is due to the off-chip broadband balun, which have a much smaller phase and amplitude difference at higher frequencies.

Fig. 12 shows the input reflection coefficient measured by a vector network analyzer. There is a good input match across the entire frequency range and good agreement between simulation and measurement was observed. At 1 GHz, the measured S_{11} was -8.8 dB and fell below -10 dB after 2.1 GHz.

The complete mixer draws a total current of 23 mA from a 1.5-V supply. Fig. 13 shows the microphotograph of the chip. The complete chip size is 1 mm $\times$ 1 mm (1 $\mathrm{mm^2}$) including pads. However, the size of the mixer itself is only about 500 μm $\times$ 630 μm (0.315 $\mathrm{mm^2}$), which is highly compact.

Table I shows a comparison between this work and recently published broadband down-converters in CMOS, where the $\mathrm{NF_{DSB}}$ of [16] can be estimated by subtracting 3 dB from the results. The mixer outperforms others in terms of noise performance and linearity while still having a comparable gain. Their circuit structures are also different. This work and [14] have a current reuse structure, whereas [15] is a LNA + Mixer + TIA in cascade and [16] is a folded mixer with a folded low-noise transconductor.

IV. CONCLUSION

A new broadband low-noise mixer has been designed with the noise-cancelling technique in CMOS 0.13-μm technology. The noise-cancelling technique allows broadband input matching and noise cancellation at the same time. Together with the current-bleeding technique, a high conversion gain was also achieved. Experimental results show great noise and gain performance. The mixer operates from 1 to 5.5 GHz with

an average DSB NF of 3.9 dB and a conversion gain of 17.5 dB. Broadband input matching was achieved with an average S_{11} of -11.9 dB. Due to the noise-cancelling transconductors, the mixer is able to have good performance in terms of linearity, with an IIP3 of $+0.84$ dBm at 5 GHz, despite its high gain. The mixer is also very compact, where the core of the mixer is only 0.315 mm^2.

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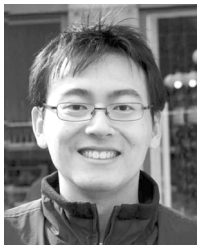

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