A Broadband CMOS Frequency Tripler Using a Third-Harmonic Enhanced Technique

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***Abstract*—A third harmonic enhanced technique is proposed to implement a broadband and low-phase-noise CMOS frequency tripler. It nonlinearly combines a pair of differential fundamental signals to generate deep cuts at the peaks of the fundamental waveform, resulting in a strong third harmonic frequency output. This mechanism has inherent suppression on the fundamental and the other harmonics so that only a low-Q high-pass filter on the lossy silicon substrate is applied at the output to further reject the fundamental and the second harmonic frequencies, in contrast to the high-Q filters used in most of the previous tripler designs. The fabricated circuit using 0.18 μm CMOS technology is compact and has an input frequency range from 1.7 GHz to 2.25 GHz, or an output frequency range from 5.1 GHz to 6.75 GHz, resulting in about 28% frequency bandwidth. The optimum conversion loss from the tripler is 5.6 dB (27.5% efficiency) at an input power of −2 dBm. The suppressions for the fundamental, second and fourth harmonics in the measurement are better than 11 dB, 9 dB, and 20 dB within an input power range from 2 dBm to 7 dBm.**

***Index Terms*—CMOS, broadband, frequency multiplication, frequency tripler.**

I. Introduction

FREQUENCY multiplication most often relies on producing signal harmonics. These harmonics are generated by exploiting the nonlinear properties of diodes or transistors, and then the interested harmonic frequency is extracted out from the harmonics using filters. For instance, a frequency doubler can be implemented using the squaring term of a diode's *I–V* characteristic. This device has been widely used in the RF/wireless systems due to its easy implementation. In contrast, a frequency tripler with a frequency multiplication ratio of three is more difficult to realize because the third harmonic frequency is far from the fundamental frequency and the nonlinear intermodulation product at that frequency is usually low compared to those at the fundamental frequency and the second harmonic frequency. Therefore, other techniques are needed to generate this triple frequency.

There are two common nonlinear techniques currently used for triplers. One is using the diode-pair method. Anti-parallel diode pairs [1]–[6] and anti-serial (back-to-back) diode pairs [7]–[11] are often used in this technique, where the diodes work as varactors. Connecting two varactors in an anti-parallel or anti-serial structure results in a symmetric nonlinear capacitance-voltage (C-V) property [7], [9], [11], which can be used to generate the triple frequency. This symmetric *C–V* property has an approximate function

$$C = aV^2 \tag{1}$$

where C and V denote the capacitance and the applied voltage, respectively, and a is usually a small constant. With the applied voltage V, the current of this capacitance can be derived by substituting the capacitance C from (1) into its expression

$$i = V/Z = j\omega CV = ja\omega V^3 \tag{2}$$

where the cube of the voltage V indicates that the third harmonic and the fundamental will equally dominate the output current, if the voltage V is a fundamental sinusoidal signal. The even harmonics generated by each varactor are cancelled by the above symmetric *C–V* property. Thereafter, the fundamental has to be rejected at the output and the third harmonic rejected at the input, by applying an output filter and an input filter, respectively. There are some higher-order odd harmonics than the third one, but they are negligible due to their small amplitude. Although these diode pairs can be implemented on most semiconductor technologies, their conversion efficiency is generally lower than 10% [2], [3], due to the reduced capacitance-voltage variation of the diode pairs [7]. In addition to the diode pairs, there is another specific type of device having the same symmetric nonlinear *C–V* property inherently, which is barrier varactor (BV) including single barrier varactor (SBV) [12]–[14], heterostructure barrier varactor (HBV) [15]–[22], and quantum barrier varactor (QBV) [23]–[25]. The BV devices are usually more efficient than the diode-pairs due to their sharper symmetric nonlinear *C–V* property [12], [16], [24], which makes them suitable for implementation of frequency triplers. However, specialized fabrication processes are required to fabricate these devices, which prevents them from being integrated with other circuits using commercial technologies.

The other common technique used to generate the triple frequency is using overdriven devices, such as overdriven HEMT transistors [26]–[33]. When a single-ended transistor is overdriven by a large input signal, the clipping occurs at each peak of the output waveform. It results in a waveform similar to a square wave, which contains a large fundamental product and other odd harmonics including the expected third harmonic. To improve the efficiency of this kind of tripler circuit, the transistor can be biased for Class AB or Class B operation [26], [27]. Filters are also needed in this kind of tripler circuit to reject the unwanted fundamental/harmonic products both at the

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output and the input. Some balanced structures based on couplers and two identical overdriven amplifiers could be an alternative to the filters to suppress the unwanted frequency products [34], [35], but with no benefit on size and efficiency because of the large-size couplers and the doubled DC power consumption. Besides the above configurations, some other overdriven configurations, such as differential bipolar transistor pair [36] and cascode differential bipolar transistor pair [37], were also developed.

A new technique to realize a broadband frequency tripler is proposed in this paper, which can enhance the tripler's third harmonic output as well as the suppression of the fundamental, using a relatively low-Q filter on-chip. Further filtering may be used off-chip for applications demanding significantly higher harmonic suppression. The tripler technique presented here is uniquely suited for CMOS implementation due to the novel use of both nMOS and pMOS transistors. Currently, RF silicon technologies are attracting attention owing to their unique properties: 1) low-cost and well-commercialized processes; 2) ability to integrate both digital and analog circuits, i.e., system-on-chip (SOC); 3) well-known high thermal conductivity. A 0.18 μm CMOS frequency tripler circuit using the proposed technique was fabricated, which can achieve broadband frequency output from 5.1 GHz to 6.75 GHz with low phase noise. To the best of our knowledge, this is the first high-frequency tripler demonstrated using CMOS technology.

The rest of this paper is organized as follows. The developed third harmonic enhanced technique is introduced in Section II, followed by its CMOS circuit implementation in Section III. Section IV gives the simulation and the measurement results to demonstrate this technique. Finally a conclusion is drawn in Section V.

II. Third-Harmonic Enhanced Technique

The concept of the proposed third harmonic enhanced technique is that if one can make a "deep cut" into the shape of each peak of a fundamental waveform, instead of only a "clip" at each peak in the overdriven technique, the output waveform (either voltage or current) would more resemble a triple frequency waveform than the square wave, as illustrated in Fig. 1. In Fig. 1(a) where the overdriven technique is used, the fundamental frequency still dominates the clipped waveform. Whereas in the Fig. 1(b) the fundamental waveform peaks are cut deeply into their shapes and it causes the significant enhancement of the third harmonic signal. At the same time the fundamental is reduced conversely and it can be totally removed in the ideal case, leaving only the third harmonic signal, as shown in Fig. 1(b). This relieves the requirement for high-Q filters on-chip, as usually required in the overdriven technique because its fundamental output from the overdriven devices is larger than its third harmonic by around 9.54 dB (3 times in amplitude) in theory [38]. In this work, a simple *LC* filter is used on-chip and excellent suppression results are achieved.

III. Circuit Implementation in CMOS

A compact CMOS circuit that can implement the proposed technique is shown in Fig. 2, where a fundamental input signal is combined with its inverted waveform in order to cancel its

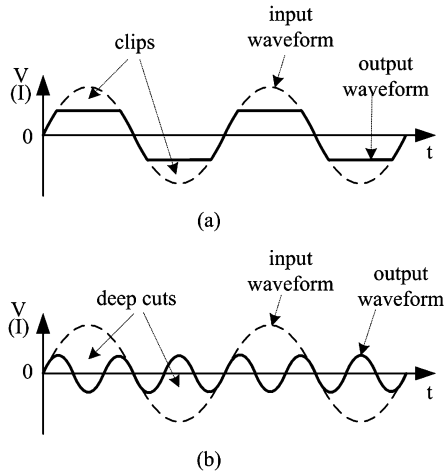


Fig. 1. Comparison between (a) the previous overdriven technique with clips and (b) the proposed third harmonic enhanced technique with ideal deep cuts.

peaks and consequently generate the deep cuts. The required inverted waveform V_2 is generated by a CMOS inverter (T_1 and T_2) in the input stage. Its input signal V_1 comes from the input signal $V_{\rm IN}$ via an input capacitor C_1 and a potentiometer composed of R_1 and R_2. The potentiometer biases the signal V_1 to a DC voltage $V_{\rm DD}/2$ to properly drive the following circuits. The input capacitor C_1 is large enough so that the signal V_1 is equal to the input signal $V_{\rm IN}$ in AC. Since the signal V_1 is fed to the gates of four MOSFETs in the following circuits with relatively high input impedance, R_1 and R_2 are simply set to both 100 Ω to achieve 50 Ω input impedance for the broadband input matching.

After the input stage, the signal V_1 and the inverted signal V_2 are fed to an inverter-type nonlinear combiner to produce the expected deep cuts, which is the core circuit of the proposed tripler. Note that the combination or cancellation of the two signals in the combiner should take effect only when the input signal is at its peaks. Therefore, some thresholds are expected from the combiner to determine when this combination/cancellation starts and stops. As shown in Fig. 2, the nonlinear combiner comprises two inverters, one with T_3 and T_6, and the other one with T_4 and T_5. T_3 and T_6 (the first inverter) are separated by the second inverter, i.e., T_3 is on its top and T_6 is on its bottom, so that the two inverters share the same current path. The first inverter (T_3 and T_6) is controlled by the input signal V_1 and has two input thresholds, ${\rm TH}_1 = V_{\rm DD} - V_{\rm TP}$ from its top pMOS (T_3) and ${\rm TH}_4 = V_{\rm TN}$ from its bottom nMOS (T_6). The second inverter (T_4 and T_5) is controlled by the inverted signal V_2 and has two similar input thresholds ${\rm TH}_2$ and ${\rm TH}_3$, which are in between the above two thresholds ${\rm TH}_1$ and ${\rm TH}_4$, and are the mechanism to control the nonlinear combination and make the deep cuts on the output current I waveform.

The operation of this nonlinear combiner is illustrated in Fig. 3, where its two voltage inputs with their thresholds and its output current I are given in Fig. 3(a), (b), and (c), respectively. As illustrated in Fig. 3(a), the signal V_1 swings in between its two thresholds ${\rm TH}_1$ and ${\rm TH}_4$, therefore, both the pMOS T_3 and the nMOS T_6 for the first inverter are turned on and they work together as a transconductance controlled by their input

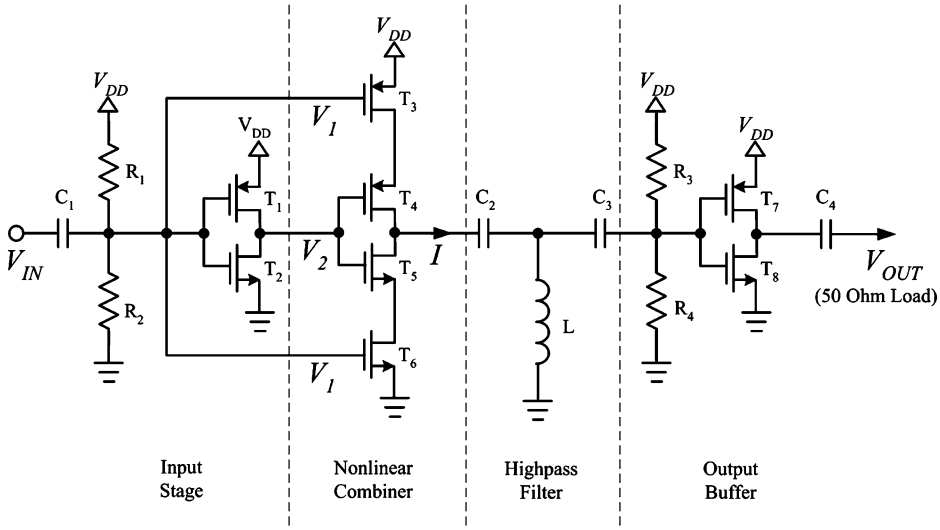


Fig. 2. Circuit implementation using CMOS technology.

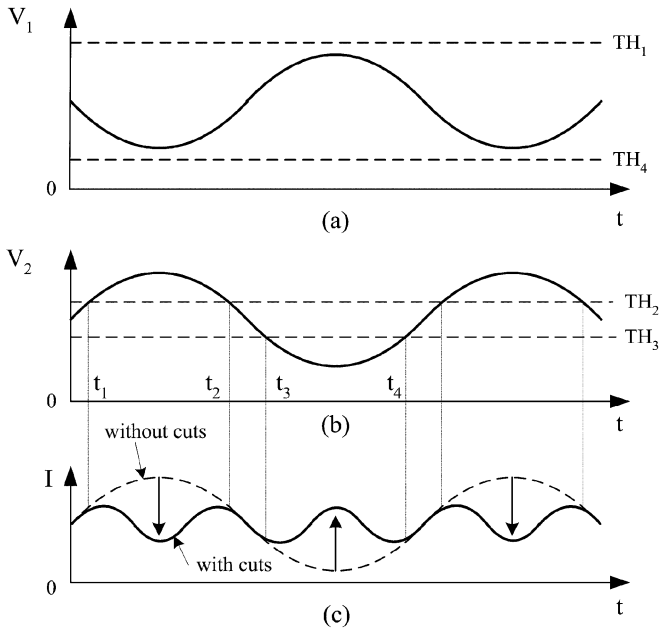


Fig. 3. Process to make the deep cuts: (a) the input fundamental waveform V_1, (b) the inverted waveform V_2, and (c) the nonlinear combination of the input waveform and the inverted waveform.

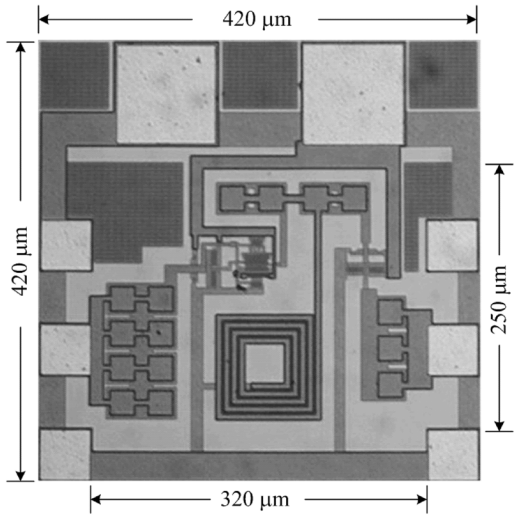
V_1 at all time. Whereas for the second inverter (T_4 and T_5), from time 0 to t_1, its input signal V_2 swings in between its two thresholds TH_2 and TH_3, so it also works as a transconductance, but inverse to the first one because of its inverted input. In order not to cancel the first transconductance, the size of the second inverter is set to be much larger than that of the first one. The total transconductance during this period is then mainly determined by the smaller inverter, i.e., the first inverter, since they are connected in series. Therefore, the output current I will follow the first inverter's input V_1 to go up within this time slot. From time t_1 to t_2, the signal V_2 goes over the threshold TH_2, so the pMOS T_4 of the second inverter is completely turned off while its nMOS T_5 is completely on. This decreases the output current I, as illustrated by the vertically downward arrow in Fig. 3(c). A deep cut is then produced there if it is compared to the waveform without cuts (dash line) in Fig. 3(c). From time t_2 to t_3, the second inverter returns to the complete ON state since its input V_2 is in between the two thresholds TH_2 and TH_3 again. The output current I will follow the first inverter's input V_1 during this period. Thereafter in the time slot from t_3 to t_4, its input V_2 goes below the threshold TH_3. The state of the second inverter in this time slot is reverse to that in the time slot from t_2 to t_3 : its nMOS T_5 is completely off and its pMOS T_4 is completely on. The output current I will then be increased as illustrated by the vertically upward arrow in Fig. 3(c), resulting in the other deep cut at the bottom peak in this cycle of the fundamental signal. The above process will be repeated cycle by cycle, and the third harmonic power is enhanced by the generated deep cuts in this process. The third harmonic enhancement will depend on the cut depth.

Figs. 1(b) and 3(c) show the ideal deep cuts that completely remove the fundamental in the output current I. However, the fundamental and the other harmonics usually remain there in the practical circuit due to the nonideal depth and shape of the cuts. Hence, a T-shaped *LC* high-pass filter (C_2, C_3, and L) is inserted between the nonlinear combiner and the output buffer to further reject the fundamental and the second harmonic. The output buffer is realized by simply using an inverter (T_7 and T_8) with its input biased by the other potentiometer (R_3 and R_4), in order to drive the external 50 Ω probe in the measurement. The output DC current is blocked by the capacitor C_4 to reduce the DC consumption and prevent the DC current from overdriving the external probe.

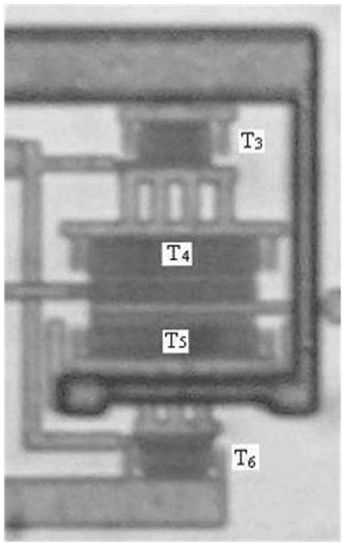
As shown in Fig. 2, the implementation of the whole tripler circuit is only based on some simple CMOS inverter-type circuits and it is thus straightforward to design. The novel use of the CMOS inverter-type circuits to create the deep cuts makes the proposed technique unique for CMOS implementation.

IV. Simulation and Experimental Results

The frequency tripler was fabricated using 0.18 μm CMOS technology to demonstrate the proposed third harmonic en-



(a)



(b)

Fig. 4. Microphotographs of the fabricated frequency tripler: (a) the whole layout and (b) the enlarged nonlinear combiner.

hanced technique. A photograph of the fabricated chip, together with its enlarged nonlinear combiner is shown in Fig. 4. Excluding the bonding pads, the tripler circuit measures only 250 μm$\times$320 μm (0.08 mm ^{2}), most of which was occupied by the capacitors and the inductor. The chip was biased at $V_{\rm dd} = 1.8$ V, resulting in a DC current of 15 mA for a DC power consumption of 27 mW. In the nonlinear combiner [Fig. 4(b)], the size of the second inverter (T_4 and T_5) was set to be 2.5 times that of the first inverter (T_3 and T_6), so that it will not affect the transconductance of the first inverter when it is in complete ON state, as detailed in Section III. In order for the tripler to work in an input frequency range at about 2 GHz, the on-chip T-shaped *LC* high-pass filter was designed to have its 3 dB cutoff frequency at 2.8 GHz as shown in Fig. 5. The spiral inductor in the filter had a value of 2 nH and was designed and analyzed using the RF CAD tool, ASITIC, resulting in a Q factor of 2.6 at 2 GHz, a relatively small value due to the lossy silicon substrate. The filter's suppression at 2 GHz in this

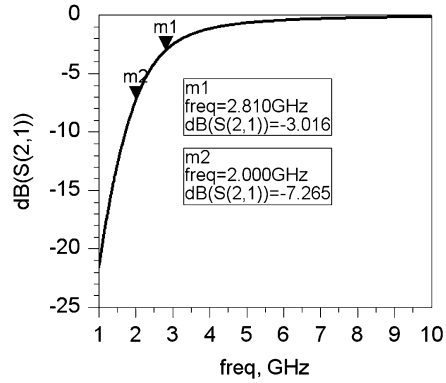


Fig. 5. Simulated characteristic of the T-shaped *LC* high-pass filter.

simulation was about 7.3 dB. The input reflection of the tripler circuit in the measurement was flat and below -10 dB within an input frequency range from 1.7 GHz to 3 GHz.

To demonstrate the operation of the fabricated frequency tripler, a 50 GHz Tektronix TDS8000 digital sampling oscilloscope was used to measure the input/output waveforms. The measured waveforms together with the simulated waveforms are presented in Fig. 6 for comparison. The simulated input waveform was identical to the measured input waveform, so only one of them is shown here [Fig. 6(a)]. In the waveform measurement two power splitters were used to split the input power for the triple's input, the oscilloscope's input and its trigger signal. The output of the tripler was then connected to the other input of the oscilloscope. The losses of the power splitters and the cables were pre-measured and included as the external losses in the oscilloscope to correct the measured waveforms, so Fig. 6(a) and (c) show the exact waveforms at the input and output of the tested tripler, respectively, where the power related to the input waveform was about 4 dBm. It can be noted in Fig. 6 that there was third harmonic product generated and dominating the output waveform both in the simulation and in the measurement. Comparison between Fig. 6(b) and (c) shows that there was very close third harmonic output power between the simulation and the measurement.

In order to verify the frequency range in which the tripler circuit can work, the output's fundamental and different harmonic powers versus the input frequency were measured and shown in Fig. 7. The input power in this measurement was set to be constant 8 dBm. The third harmonic output power varied from -4.64 dBm to -2.25 dBm, a relative flat curve within a frequency range from 5.1 GHz to 6.75 GHz or a corresponding input frequency range from 1.7 GHz to 2.25 GHz, leading to a broadband operation of about 28% frequency bandwidth. The maximal third harmonic output power (-2.3 dBm) occurred at 1.92 GHz, which is close to the designed frequency of 2 GHz, and was used for the waveform simulation/measurement described above. A higher-frequency simulation of the tripler was further carried out, which indicated the proposed tripler concept can work up to an input frequency of 4 GHz, or an output frequency of 12 GHz with appropriate filtering. The time delay of the inverter at the input stage is considered as the main reason for the frequency limit, because it affects the phase difference of the two inputs of the nolinear combiner. More precisely, the

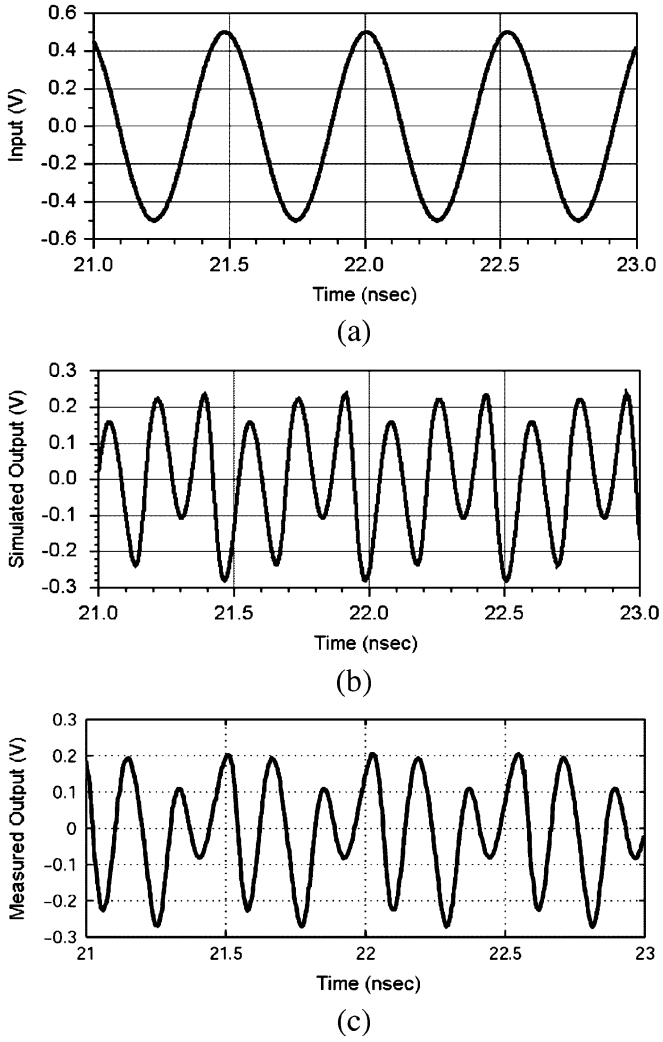


Fig. 6. (a) Simulated/measured input waveform. (b) Simulated output waveform. (c) Measured output waveform.

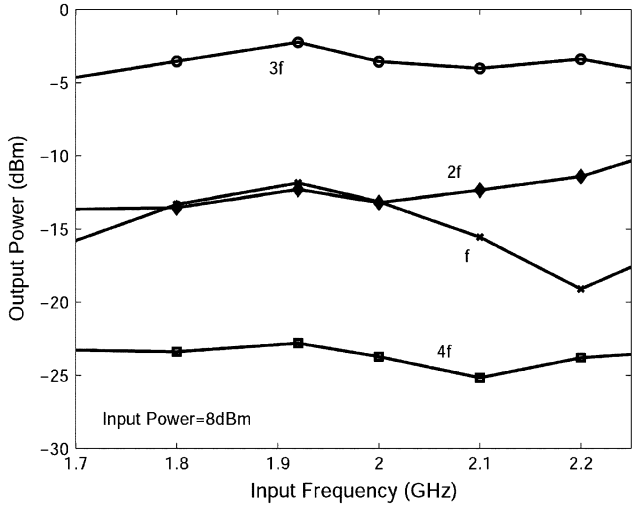


Fig. 7. Measured output powers at the third harmonic and the other frequencies versus the input frequency.

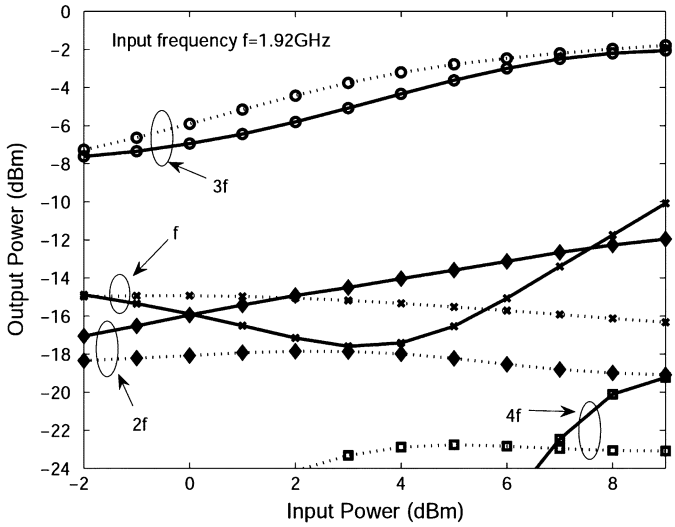


Fig. 8. Simulated (dot lines) and measured (solid lines) harmonic output powers versus the input power at 1.92 GHz.

inputs to the nonlinear combiner need to arrive at the correct phases so that the deep cuts occur at the required points of the fundamental signal.

The phase noise of the fabricated tripler was also investigated and it shows low phase-noise performance of the proposed tripler. The measurement at 1.92 GHz showed an output phase noise of -84.14 dBc/Hz for an input phase noise of -93.89 dBc/Hz, both at 20 kHz offset. The resulting phase noise degradation of 9.75 dB is very close to the theoretical minimum phase noise degradation from an ideal frequency tripler, which is 9.54 dB. The theoretical minimum degradation is given by $20\log_{10}(N)$, where N refers to the multiplication order and equals 3 for a frequency tripler [27].

Fig. 8 shows the output powers versus the input power at the input frequency 1.92 GHz, from both the simulation and the measurement. A comparison between the simulation and the measurement shows their close results for the third harmonic output power (3f). The optimum conversion loss from the tripler was 5.6 dB (27.5% efficiency) at an input power of -2 dBm. The conversion loss was less than 9.5 dB (efficiency $> 11.2\%$) for input powers up to 7 dBm. When the input power exceeded 7 dBm, the third harmonic output power saturated at around -2 dBm from both the measurement and the simulation. The suppressions for the fundamental, the second and fourth harmonics in the measurement were better than 11 dB, 9 dB, and 20 dB within an input power range from 2 dBm to 7 dBm. The best harmonic suppression occurred at 4 dBm input, where the suppressions for the fundamental, the second and fourth harmonics in the measurement were 13 dB, 10 dB, and 33 dB, respectively. Among the fundamental, second and fourth harmonic output powers, the fourth harmonic was the lowest one and was roughly predicted by the simulation. The fundamental and the second harmonic output powers from the simulation were close to those from the measurement at low input power, but deviated from them when the input power increased. This deviation was considered as a result of the increased temperature in the tested chip as the input power increased, which the simulator cannot accurately model.

From the above measurement, if the fundamental suppression of the T-shaped filter (around 8 dB at 1.92 GHz) was removed, the nonlinear combiner itself in the fabricated tripler has a maximal 5 dB fundamental suppression. The gain of the output buffer was assumed to be constant across the frequency band in the above calculation. However, the fundamental suppression of the nonlinear combiner could be higher than 5 dB because the output buffer actually has lower gain at the third harmonic frequency than that at the fundamental, which reduces the total fundamental suppression of the tripler circuit. Comparing with the diode-pair tripler technique [1]–[11] and the overdriven-transistor tripler technique [26]–[37], in which the former has a third harmonic product equal to the fundamental (0 dB fundamental suppression) and the later has even a third harmonic product 9.54 dB lower than the fundamental one (−9.54 dB fundamental suppression) without filters, the result from the nonlinear combiner presented in this work reveals a significant enhancement of the third harmonic signal compared to the above two techniques.

V. Conclusion

The proposed third harmonic enhanced technique is suitable for implementation in silicon CMOS technologies. The third harmonic enhancement from the nonlinear combiner is significant compared to that from the overdriven techniques. Its broadband, low phase noise, and low conversion loss properties make it especially attractive to realize tunable high-frequency sources using CMOS processes. Moreover, the size of this tripler circuit is small compared to the other MMIC tripler circuits, where transmission lines proportional to wavelength were usually employed in their filters.

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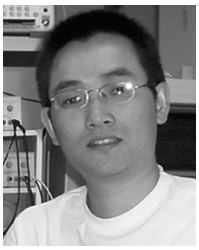

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