Ring-Hybrid Microwave Voltage-Variable Attenuator Using HFET Transistors

Carlos E. Saavedra, *Senior Member, IEEE,* and You Zheng, *Student Member, IEEE*

***Abstract*—In this paper, a voltage-variable microwave attenuator circuit is presented. The input signal first enters a rat-race power splitter where a 0° and a 180° pair of signals is generated. The 0° signal passes through a common-gate field-effect transistor (FET) that is fully turned on, with its gate voltage set to 0 V. The 180° signal enters another common-gate transistor biased in the triode region. By changing the gate voltage of the second FET, the amplitude of the 180° signal is varied. The in-phase and out-of-phase signals are summed at the output and variable attenuation is achieved. The concept was demonstrated experimentally from 3.0 to 3.4 GHz and a variable attenuation from 6 to 30 dB was achieved. The phase response is linear over the frequency band and exhibits a group delay of 0.71 ns. The input 1-dB compression point of the attenuator is 0 dBm and the second harmonic suppression is 18.5 dB at 0-dBm input power.**

***Index Terms*—Attenuator, common-gate transistor, power combiners, power splitters, variable attenuator.**

I. Introduction

Attenuator circuits are frequently used in microwave communications systems in order to bring the gain of a transceiver within a specified window. This is because, in many instances, the amplifiers used in the system have a fixed gain and these gains do not exactly sum up to the required overall gain. Other applications of attenuators include RF source power control, and beam-forming networks [1].

Obtaining a fixed attenuation value is a relatively simple task and it can be accomplished using a resistive T-network [2], π-network, or bridged-T network. Other fixed attenuators have been proposed using asymmetric rat-race couplers [3]. In many applications, however, what is needed is a variable attenuator whose attenuation can be electronically changed over a specified range. Such circuits make it possible to have very precise transceiver gain control over frequency and temperature if the voltage versus attenuation characteristic is programmed into a microcontroller.

To date, a variety of voltage-variable attenuator (VVA) circuit implementations have been demonstrated. Some VVAs, particularly the integrated-circuit (IC) versions, are derived from the basic lumped-element resistive topologies using T, bridged-T, or π-networks of transistors [4]. In those designs, the reflection coefficient of the VVA is generally small since the incident signal is absorbed by the network. The circuit in [4] has an attenuation range of 28 dB from dc to 900 MHz. In [5], a bipolar-based variable attenuator is demonstrated at low RF frequencies, which exhibits an attenuation of 0–25 dB. Some attenuators use transmission lines with p-i-n diodes in shunt [6]. By changing the bias voltage of the diode, the equivalent resistance to ground changes and the incident signal can be attenuated. The attenuator in [6] exhibits an overall attenuation range from 6 to 35 dB, and a linear attenuation from 12 to 28 dB reported at a single frequency of 12.5 GHz. A different VVA implementation works on the reflection principle [7]. In that approach, a branch-line coupler is used to split the incoming signal into in-phase and quadrature components. The two output ports of the coupler are terminated with varactor diodes, which reflect the incident signal and the waveforms destructively interfere back at the isolated port, which is now the output. By changing the bias voltage of the varactor diodes, the amplitude of the reflected signals vary and variable attenuation is achieved. The circuit in [7] has an attenuation range of 2.2–17 dB over a frequency span of 2.8 to 4.2 GHz. A monolithic counterpart of the reflection-type amplifier is described in [8] and it has an attenuation range from 1 to 14 dB from 8 to 12 GHz.

In this paper, a new concept for a VVA is presented. The circuit consists of a ring hybrid, two field-effect transistors (FETs), and a 0° Wilkinson power combiner. The circuit exhibits an overall attenuation range from 6 to 30 dB over a 13% bandwidth. The attenuator can achieve high attenuation values with low harmonic distortion. At 10-dB attenuation, the second harmonic is 18.5 dB below the fundamental. Furthermore, the attenuator has a simple bias circuit and it is easily modeled. This paper is organized as follows. Section II describes the operation of the circuit. Section III presents the calculated and experimental results. Section IV concludes this study.

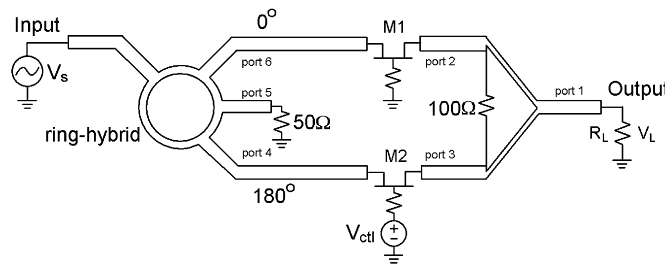

Fig. 1. VVA circuit using series HFET transistors.

II. Variable Attenuator Circuit

A circuit diagram of the proposed VVA is shown in Fig. 1. The incident signal enters the ring hybrid, where it is equally split into in-phase (0°) and out-of-phase (180°) components.

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The authors are with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada K7L 3N6 (e-mail: carlos.saavedra@queensu.ca).

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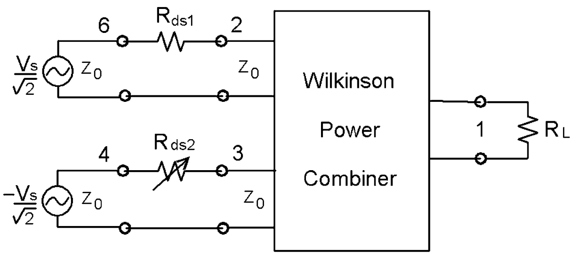

Fig. 2. VVA model.

The in-phase signal passes through the transistor M_1, which is fully turned on by setting its gate voltage to 0 V. The series resistance presented by M_1 is very small so that the signal propagates through the device with minimal loss. The out-of-phase signal enters the second transistor M_2, whose gate terminal is connected to a control voltage $V_{\rm ctl}$. Transistor M_2 operates in the triode region and, thus, it behaves as a voltage-controlled resistance: as the control voltage $(V_{\rm ctl})$ changes, the amplitude of the signal passing through M_2 changes because the drain-to-source resistance of the transistor varies. When the signals emerging at the drains of M_1 and M_2 are added using the 0° Wilkinson power combiner, attenuation takes place. Maximum attenuation occurs when both transistor gates are at 0 V, and minimum attenuation when the gate of transistor M_2 is well below its threshold voltage so that it is fully turned off. The minimum attenuation of this circuit is 6 dB because the ring hybrid generates a 3-dB power split and the Wilkinson generates another 3-dB power split when device M_2 is off (infinite drain–source resistance). In principle, the presence of transistor M_1 would seem redundant since that device is always turned on and the loss through it is small. However, when transistor M_2 is fully turned on, the signal passing through it experiences a nonzero phase shift. Therefore, the same phase shift should be present on the top-half of the circuit so that the top and bottom signals cancel each other correctly and without distortion. Thus, the need for transistor M_1.

To mathematically model the attenuation versus control voltage characteristic of this circuit, one can use the simplified circuit model shown in Fig. 2. If the input signal to the attenuator is Vs, then the ring hybrid will generate two signals with equal amplitude and opposite phase or $Vs/\sqrt{2}$ and $-Vs/\sqrt{2}$. These two signals encounter two series resistances $R_{\rm ds1}$ and $R_{\rm ds2}$, which are the drain-to-source resistances of transistors $M1$ and $M2$, respectively. In this model, the parasitic capacitances of the transistors are neglected without significant adverse impact on the calculated results. The resistance $R_{\rm ds1}$ is constant, while the resistance $R_{\rm ds2}$ is a function of the control voltage $V_{\rm ctl}$ because the transistor operates in the triode region. Assuming that the Wilkinson power combiner at ports 2 and 3 looks like it is perfectly matched to Z_0 and using s-parameters, the transmission coefficient through $R_{\rm ds1}$ is

$$\tau_{26} = \frac{2Z_0}{R_{\rm ds1} + 2Z_0} \tag{1}$$

where Z_0 is the characteristic impedance of the system. The transmission coefficient through $R_{\rm ds2}$ is

$$\tau_{34} = \frac{2Z_0}{R_{\rm ds2} + 2Z_0}. \tag{2}$$

In arriving at (1) and (2), it is approximated for simplicity that there is perfect isolation between the two output ports 4 and 6 of the 180° ring hybrid. In this manner, the voltage generated at port 6 due to the changes in the impedance at port 4 due to $R_{\rm ds2}$ are ignored. In spite of this simplification, our modeled results agree well with measurements and simulations.

The scattering matrix of a Wilkinson power combiner is

$$S = \begin{bmatrix} 0 & -\frac{j}{\sqrt{2}} & -\frac{j}{\sqrt{2}} \\ -\frac{j}{\sqrt{2}} & 0 & 0 \\ -\frac{j}{\sqrt{2}} & 0 & 0 \end{bmatrix} \tag{3}$$

from which it is evident that the signal emerging at port 1 (the output port in Fig. 2) is given by

$$b_1 = -\frac{j}{\sqrt{2}}(a_2 + a_3), \tag{4}$$

where a_2 and a_3 are the signals incident at ports 2 and 3 and b_1 is the output signal. For the circuit in Fig. 2, note that a_2 and a_3 have opposite signs because these signals come from the two output ports of the 180° ring hybrid. Therefore, the output signal is

$$b_1 = \frac{V_L}{\sqrt{Z_0}} = -\frac{j}{\sqrt{2}}\left(\frac{V_s}{\sqrt{2}\sqrt{Z_0}}\tau_{34} - \frac{V_s}{\sqrt{2}\sqrt{Z_0}}\tau_{26}\right). \tag{5}$$

Using (5), the voltage attenuation α from input to output for this circuit is (in decibels)

$$\alpha = 20\log\left|\frac{V_L}{V_s}\right| = 20\log\left|\frac{1}{2}(\tau_{34} - \tau_{26})\right| \tag{6}$$

The equivalent RF drain–source resistance $R_{\rm ds}$ of the GaAs heterostructure field-effect transistors (HFETs) is given by

$$R_{\rm ds} = (dI_{\rm ds}/dV_{\rm ds})^{-1} \tag{7}$$

where $V_{\rm ds}$ is the drain–source voltage drop and $I_{\rm ds}$ is the drain–source current. Using the TriQuint model (TOM) for FET devices, the drain–source current is [9], [10]

$$I_{\rm ds} = \frac{I_{\rm dso}}{1 + \delta V_{\rm ds} I_{\rm dso}} \tag{8}$$

where

$$I_{\rm dso} = \beta(V_{\rm gs} - V_t)^Q \cdot \left[1 - \left(1 - \frac{\xi V_{\rm ds}}{3}\right)^3\right] \tag{9}$$

$$V_t = V_{to} - \gamma \cdot V_{\rm ds} \tag{10}$$

and δ is the output feedback coefficient, β is the transconductance coefficient, $V_{\rm gs}$ is the gate–source voltage (equal to $V_{\rm ctl}$ here), V_t is the threshold voltage, V_{to} is the nonscalable portion of threshold voltage, γ is the ac pinchoff change with $V_{\rm ds}$, Q is the power law exponent, and ξ is the saturation voltage coefficient.

The above TOM equation covers the depletion region and is suitable for small-signal modeling. Substituting (9) into (8)

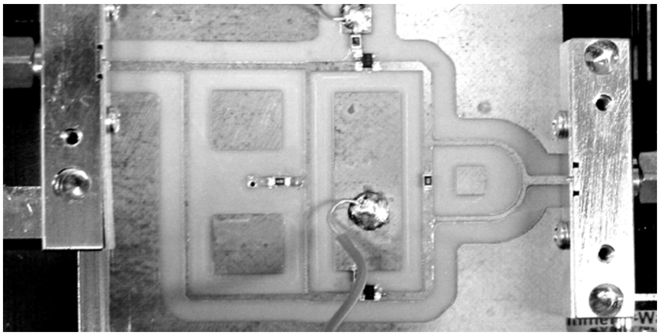

Fig. 3. Fabricated attenuator.

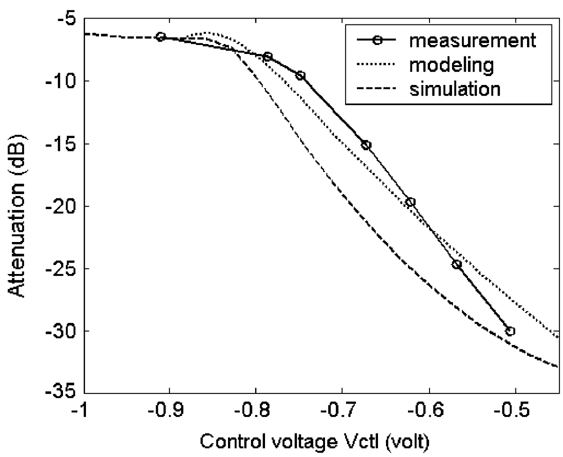

Fig. 4. Measured, calculated, and simulated (ADS) attenuation versus control voltage at 3.24 GHz.

and then differentiating according to (7) yields the equivalent drain–source resistance in the depletion region

$$R_{\mathrm{ds}} = \frac{(1+\delta V_{\mathrm{ds}} I_{\mathrm{dso}})^2}{I'_{\mathrm{dso}}(1+\delta V_{\mathrm{ds}} I_{\mathrm{dso}}) - \delta I_{\mathrm{dso}}(I_{\mathrm{dso}} + V_{\mathrm{ds}} I'_{\mathrm{dso}})} \tag{11}$$

where $I'_{\mathrm{dso}} = dI_{\mathrm{dso}}/dV_{\mathrm{ds}}$ is calculated from (8) and (9).

III. Results

The proposed VVA was fabricated using a substrate with a relative dielectric constant of 3.2 and a thickness of 0.50 mm. A photograph of the microstrip circuit is shown in Fig. 3. A milling machine was used to pattern the circuit board. The ring hybrid has a rectangular geometry and it was designed for a center frequency of 3.24 GHz. The transistors used were packaged devices (NE34018CT) from NEC, Tokyo, Japan.

Fig. 4 shows the measured, calculated, and simulated (using ADS) attenuation of the VVA circuit at 3.24 GHz versus the gate control voltage V_{ctl}. The results show that, as expected, the minimum attenuation is 6 dB. The maximum attenuation measured was 30 dB.

The calculated curve in Fig. 4 was determined using (5)–(10). For the calculations, the TOM model parameters used were those specified in the device data sheets, except for Q, which was set to 2.0 (ideal case), and the threshold voltage (V_t) was set to -0.85 V, which was determined experimentally from dc current–voltage measurements. The model in (7)–(9) predicts that the drain–source resistance is infinite when V_{ds} is zero and V_{gs} is above the threshold voltage. In reality, the resistance is finite since there is a drain–source channel induced. To overcome this situation, a V_{ds} of 0.1 V was used. This value was arrived at by measuring R_{ds} at dc with zero applied voltage, and then finding the value of V_{ds} that would yield the same R_{ds}. Ultimately, what one is interested in is the inverse *derivative* in

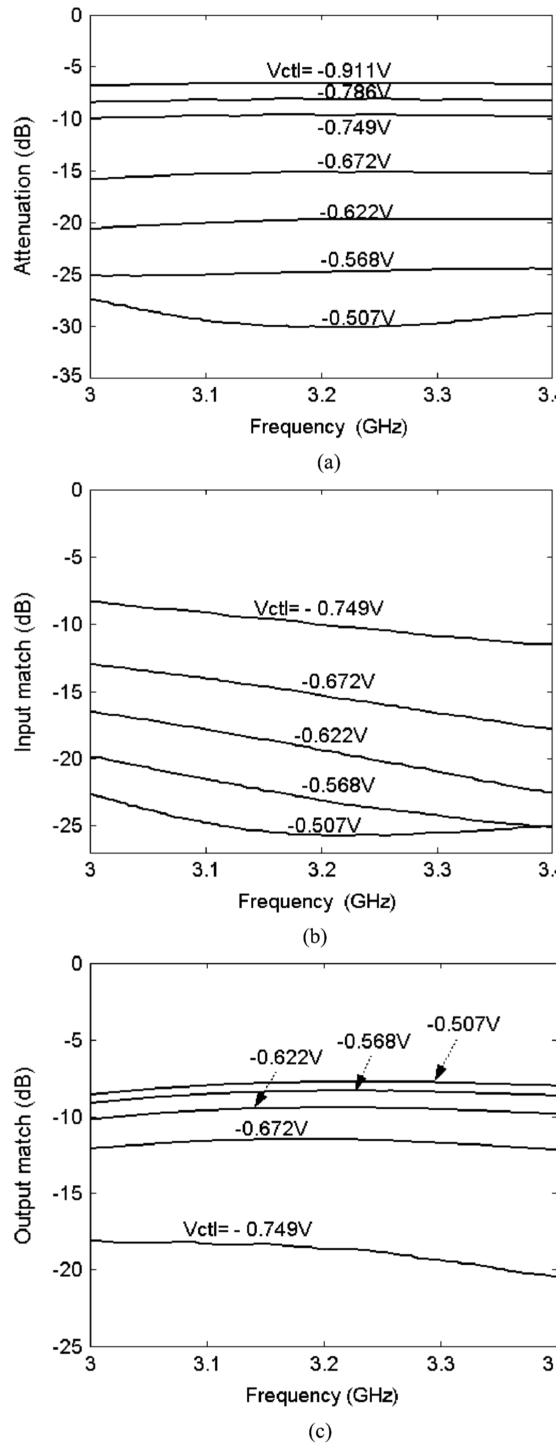

Fig. 5. (a) Attenuation, (b) input reflection coefficient, and (c) output reflection coefficient versus frequency and control voltage.

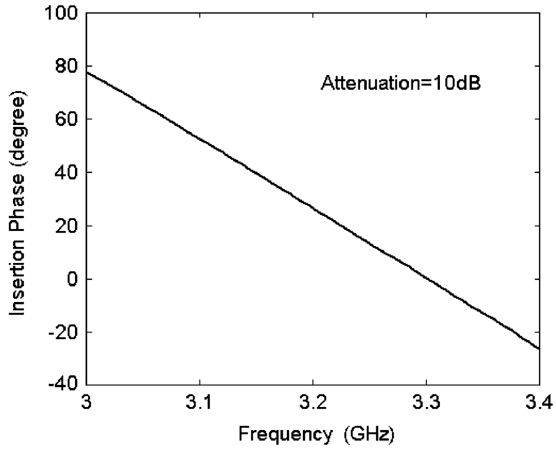

Fig. 6. Measured insertion phase shift versus frequency.

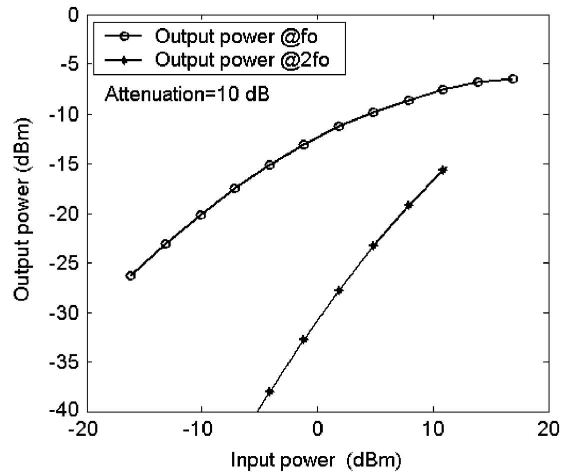

Fig. 7. Measured output power performance and harmonic generation of the attenuator.

(6), and the precise value of $V_{\rm ds}$ is not so critical as long as the transistor stays in the depletion region.

Fig. 5(a) presents the measured attenuation versus frequency and control voltage for this VVA. The attenuation is essentially constant versus frequency up to 25-dB attenuation, and then shows a moderate frequency dependence at a gate control voltage of -0.507 V, or 30-dB attenuation. The frequency span of this attenuator is 3.0–3.4 GHz, which implies a 13% bandwidth. The main factor limiting the frequency response is the phase error of the ring hybrid. At the center frequency, the hybrid produces two exactly out-of-phase signals, but as one moves away from the center, the phase difference changes and the signals do not exactly cancel out any more at the Wilkinson power combiner.

The input reflection coefficient of the VVA versus frequency was also measured for different gate control voltages in the linear attenuation region of 10–30 dB. The results are shown in Fig. 5(b). The reflection coefficient at each gate voltage slowly rolls off with frequency. More interesting is the fact that S_{11} decreases with increasing attenuation. This is the opposite of what happens in a reflection-type attenuator. The reason the reflection coefficient decreases in this VVA is because, at high attenuation, transistors $M1$ and $M2$ are both fully turned ON. Thus, there is little energy reflected back toward the input from the source terminals of $M1$ and $M2$. The output reflection coefficient of the attenuator is plotted in Fig. 5(c). It is seen that the output reflection coefficient changes in the reverse manner as the input reflection coefficient with applied control voltage.

To examine the group delay of the fabricated VVA, the insertion phase shift at an attenuation of 10 dB (corresponding control voltage $V_{\rm ctl} = -0.75$ V) was measured versus frequency, as shown in Fig. 6. The insertion phase is linear with frequency, indicating a uniform group delay of 0.71 ns through the 400-MHz bandwidth at the examined attenuation.

Fig. 7 shows the measured power performance of the attenuator. The graph shows the output power versus input power for the fundamental signal and its second harmonic. The measurements were made at an attenuation of 10 dB. The input 1-dB compression point for the attenuator is 0 dBm. The suppression of the second harmonic at 0 dBm input power is 18.5 dB.

IV. CONCLUSION

A concept for a VVA using a ring hybrid has been demonstrated. Whereas this attenuator circuit has a simple construction and is cost effective, the tradeoff occurs in the large area required due to the large size of the ring hybrid. However, this issue can be solved by using a very high dielectric-constant substrate. The circuit operates from 3.0 to 3.4 GHz and exhibits an attenuation range from 6 to 30 dB. The attenuation versus control voltage characteristic of the VVA was calculated using the TOM model, and the results agree quite well with experiment. The reflection coefficient of the VVA decreases with increasing attenuation and the phase response of the attenuator exhibits a linear dependency with frequency.

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Carlos E. Saavedra (S'92–M'98–SM'05) received the Ph.D. degree in electrical engineering from Cornell University, Ithaca, NY, in 1998.

From 1998 to 2000, he was with the Millitech Corporation, South Deerfield, MA, where he designed millimeter-wave transmitter and receiver circuits for 31-GHz local-to-multipoint distribution systems and 38-GHz point-to-point radio systems. Since August 2000, he has been an Assistant Professor with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada. His current research activities include the design of RF and microwave circuits and systems such as phase shift-keying modulators, demodulators, phase shifters, microwave filters, and phase-locked loops. His teaching interests are in the area of electronic circuits for communications applications.

Dr. Saavedra is a member of Eta Kappa Nu and Tau Beta Pi. He was the recipient of the 2001 Excellence in Teaching Award presented by the Queen's University 2002 electrical engineering class.

You Zheng (S'03) received the B.Sc. degree from Xiamen University, Xiamen China, in 2000, the M.Sc. degree in electrical engineering from Queen's University, Kingston, ON, Canada, in 2004, and is currently working toward the Ph.D. degree at Queen's University.